

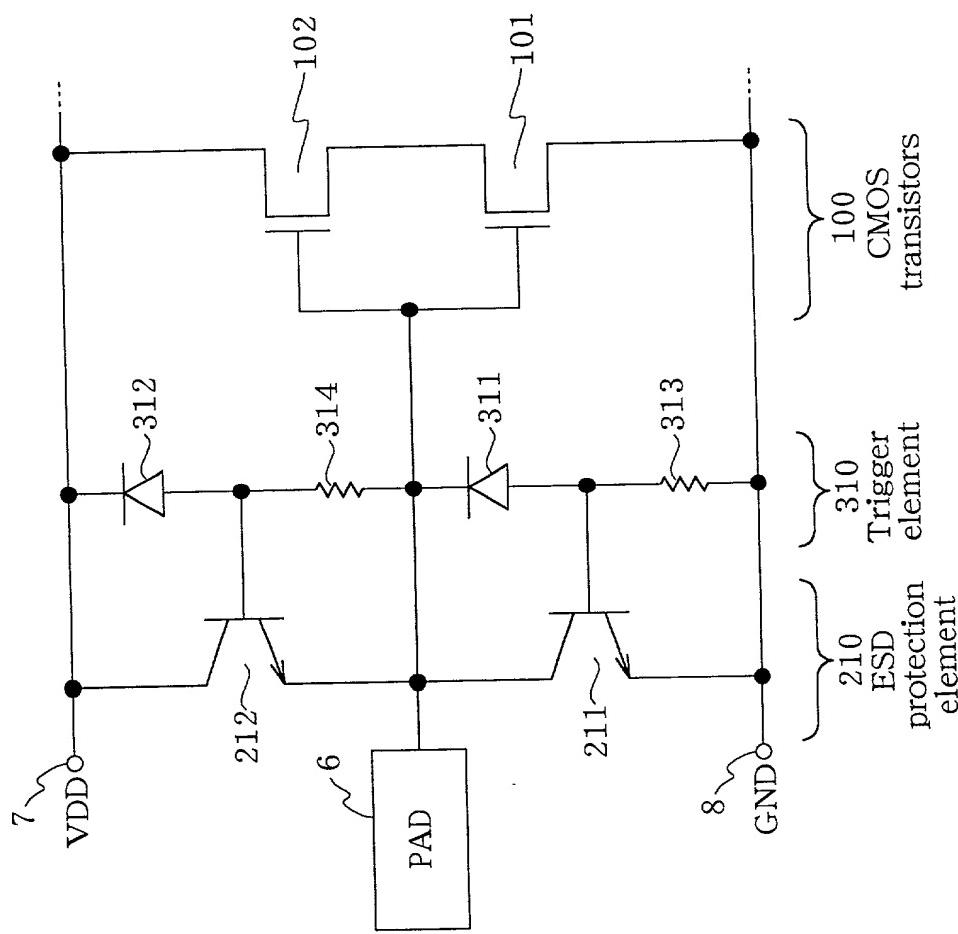
FIG. 1

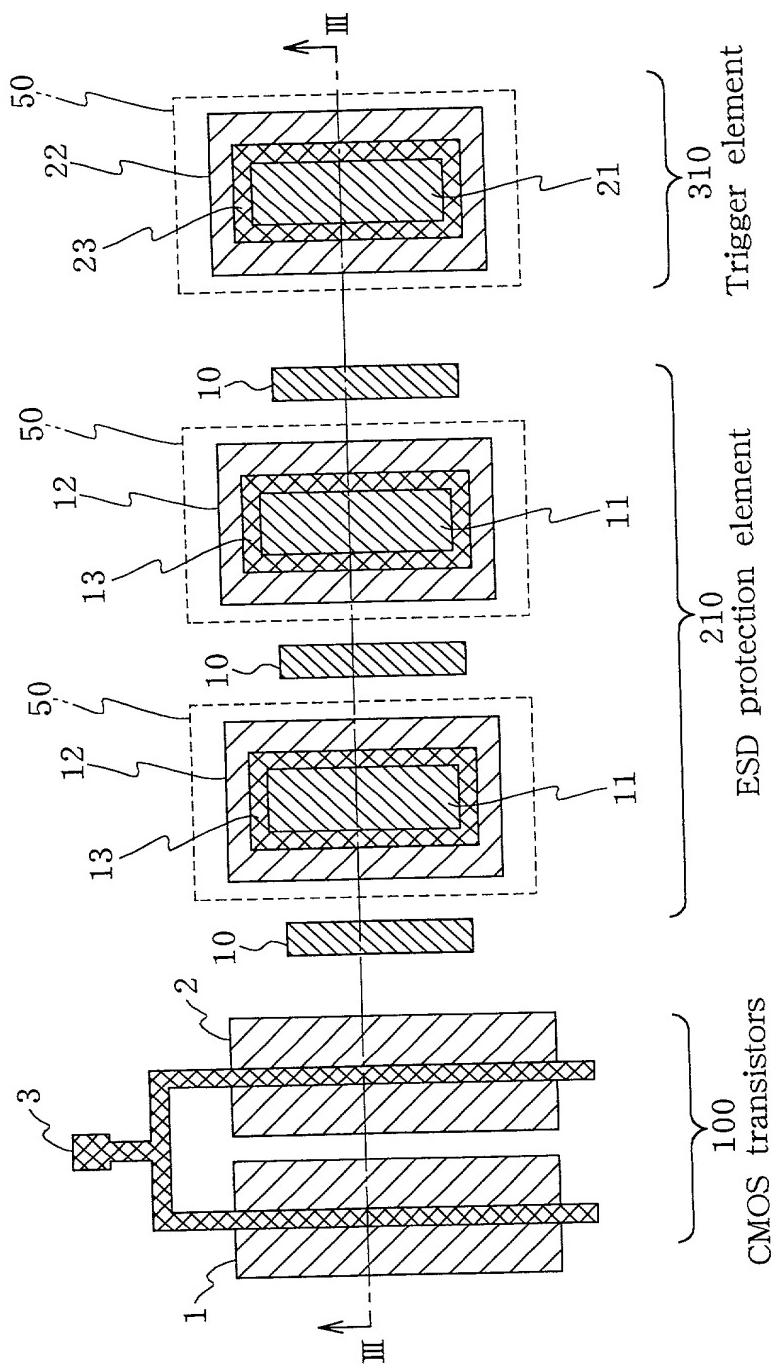
FIG. 2

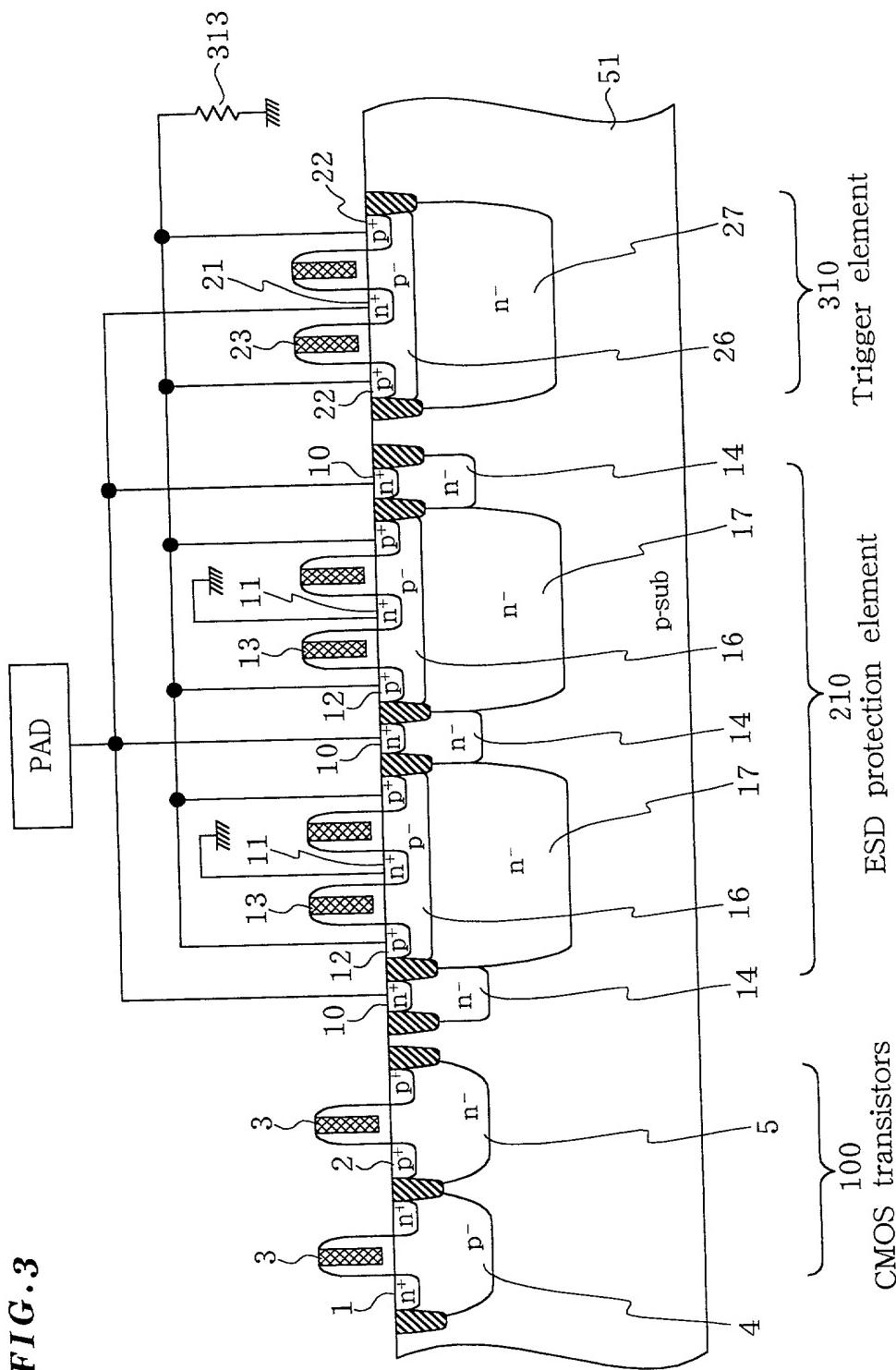
FIG. 3

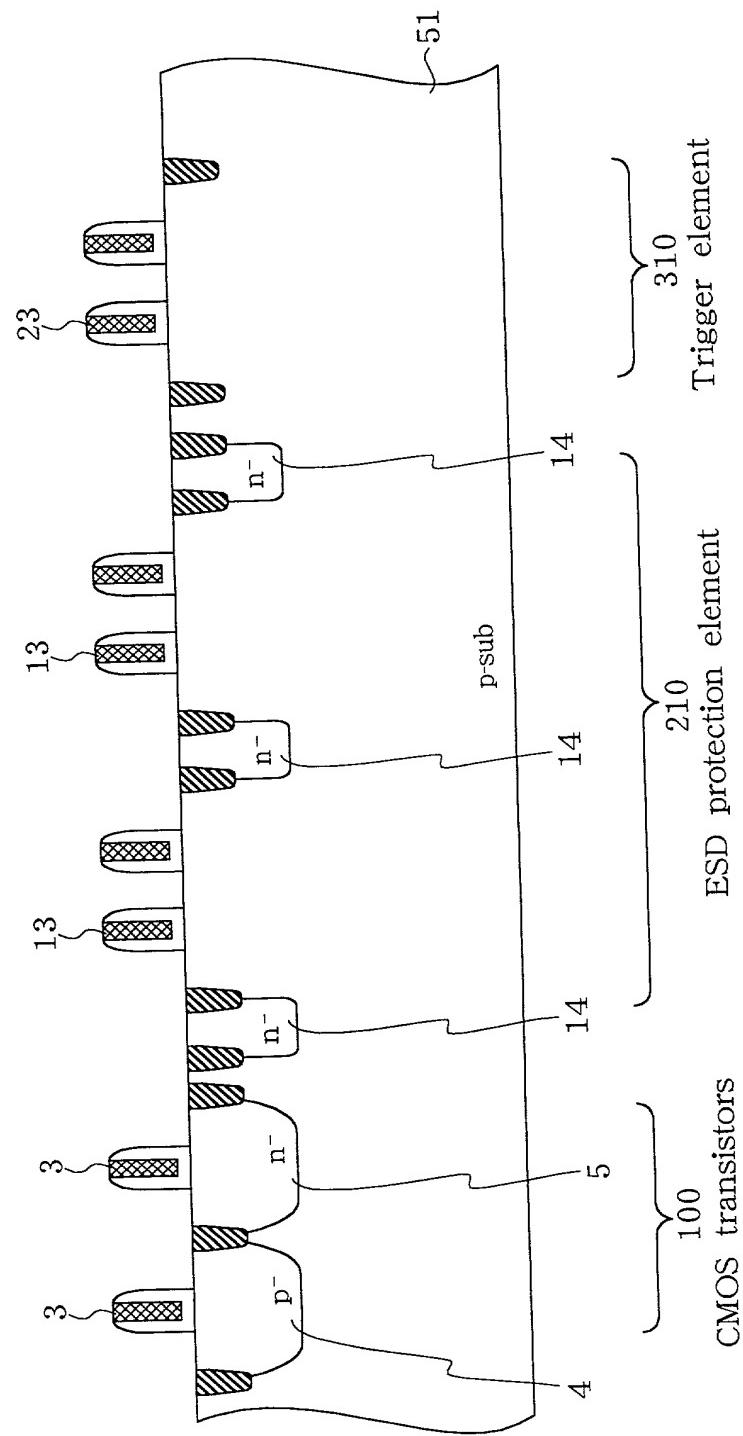
FIG. 4

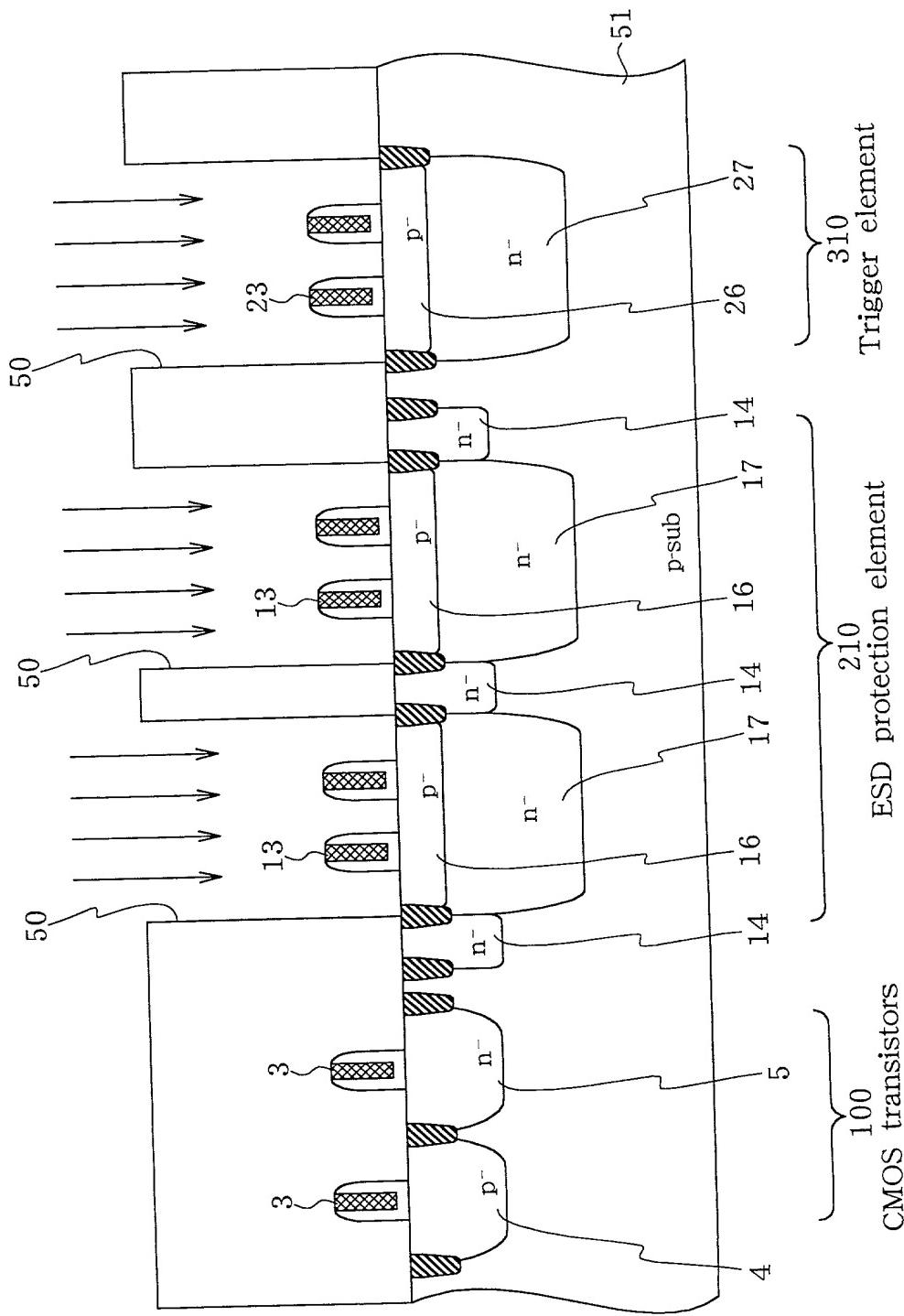
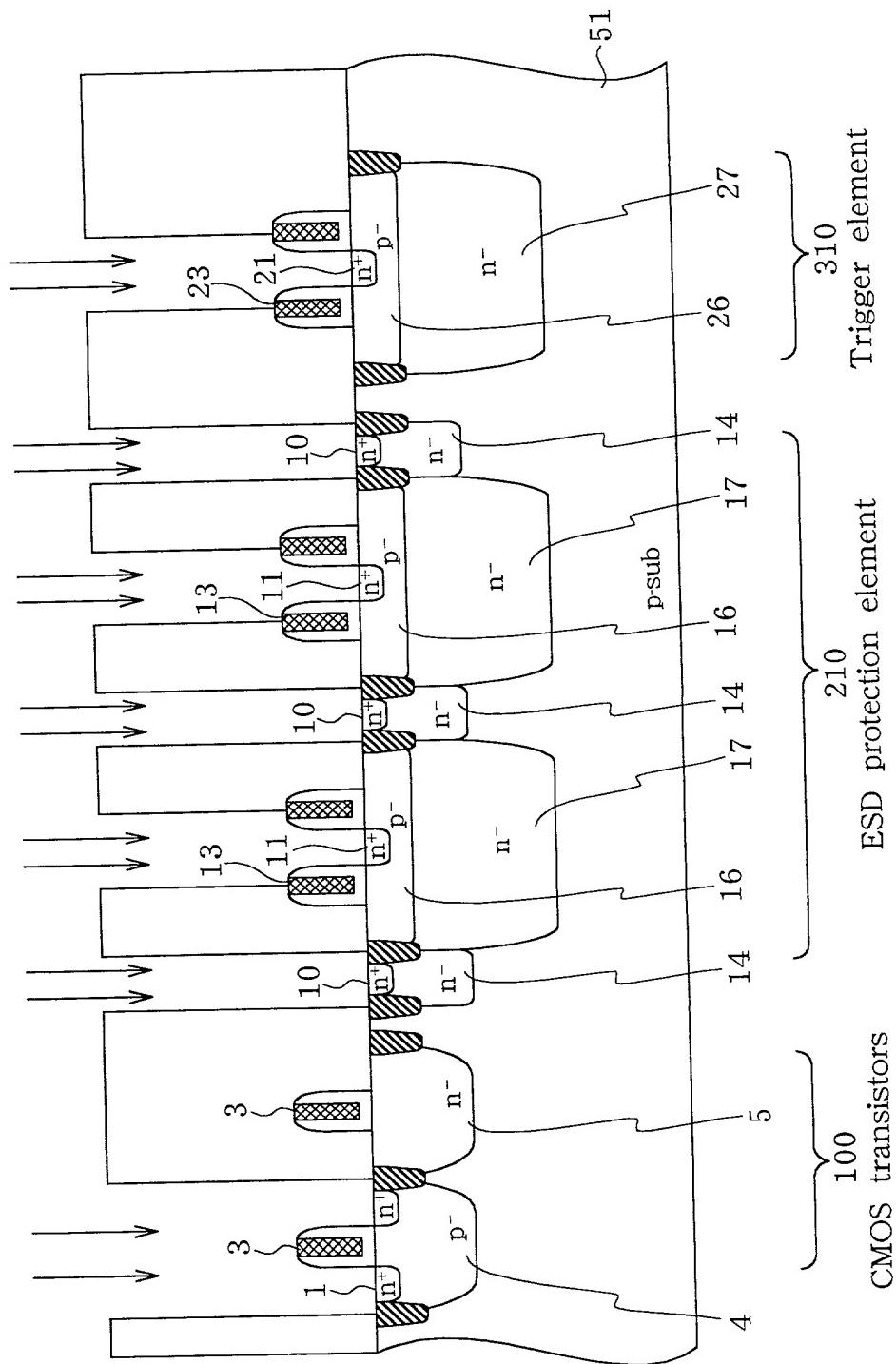
FIG. 5

FIG. 6



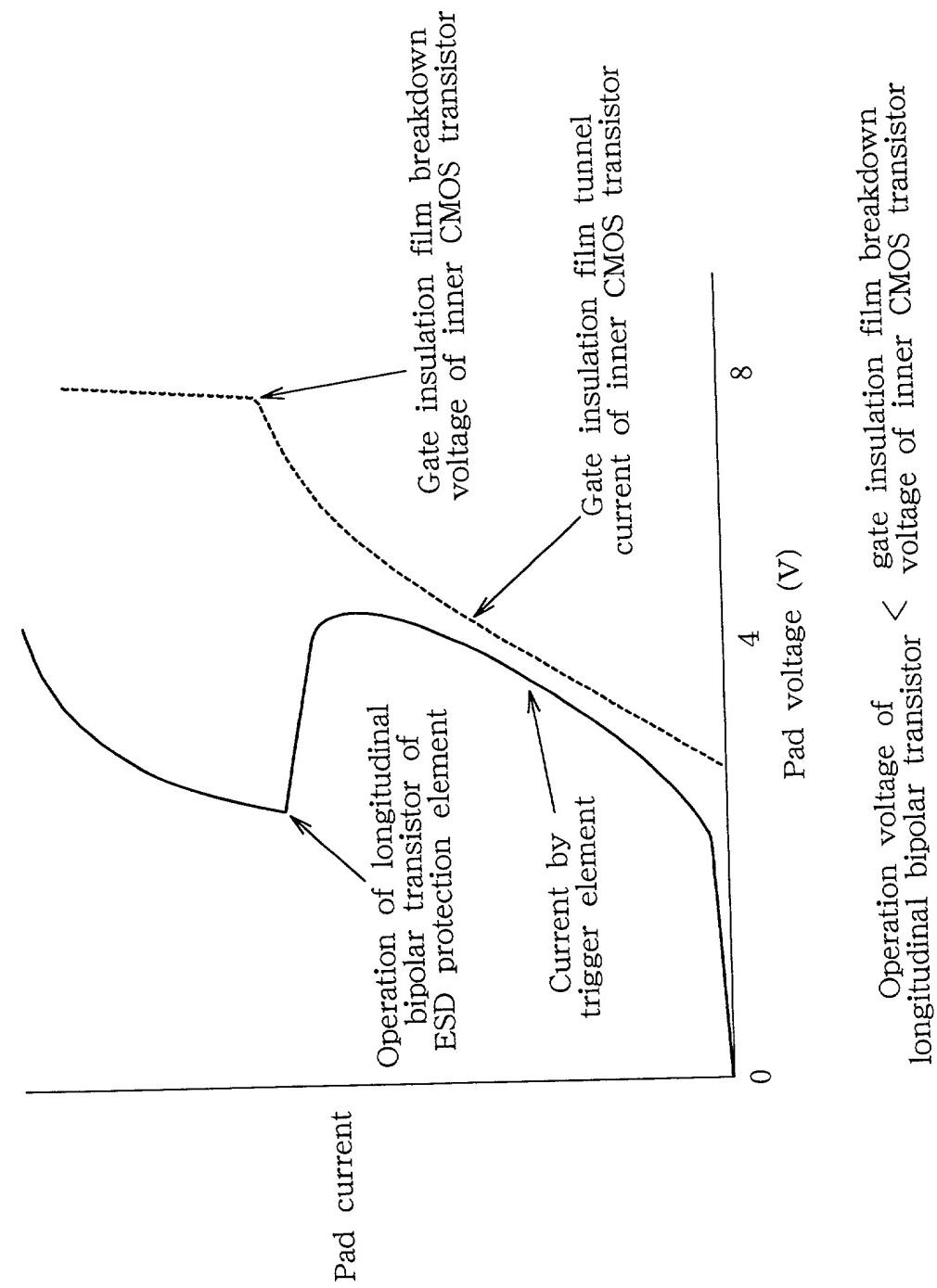
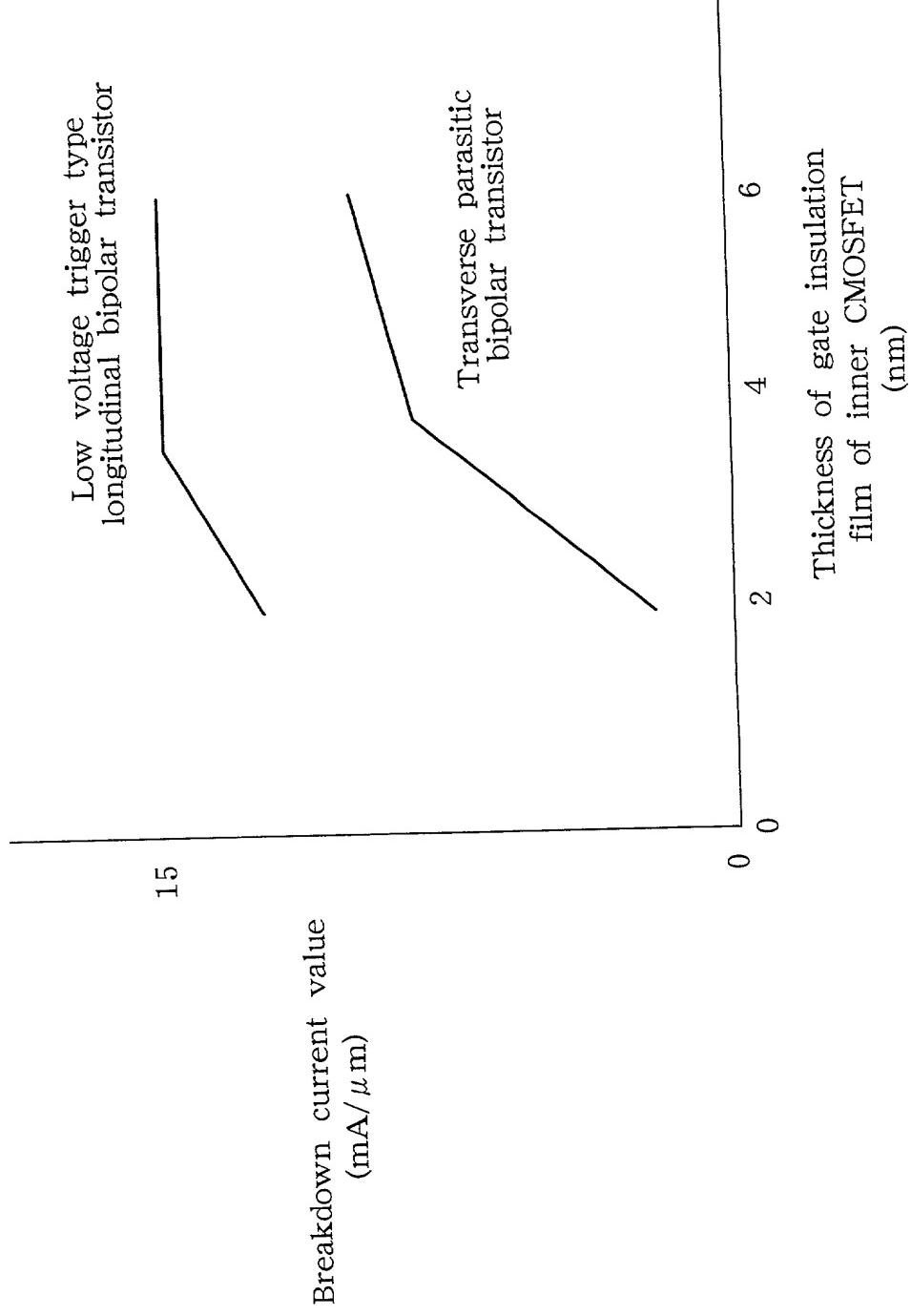


FIG.7

FIG. 8

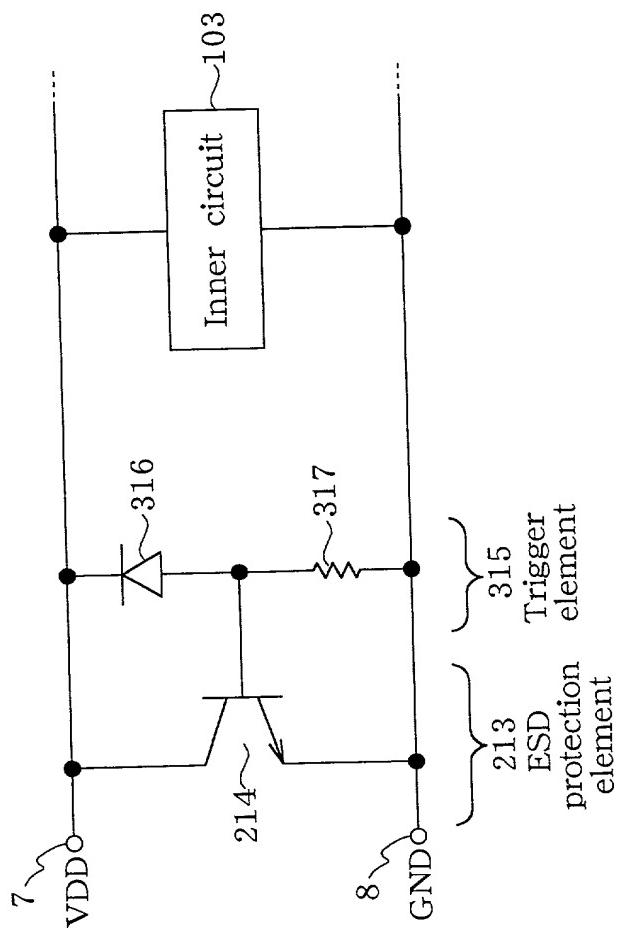


FIG. 9

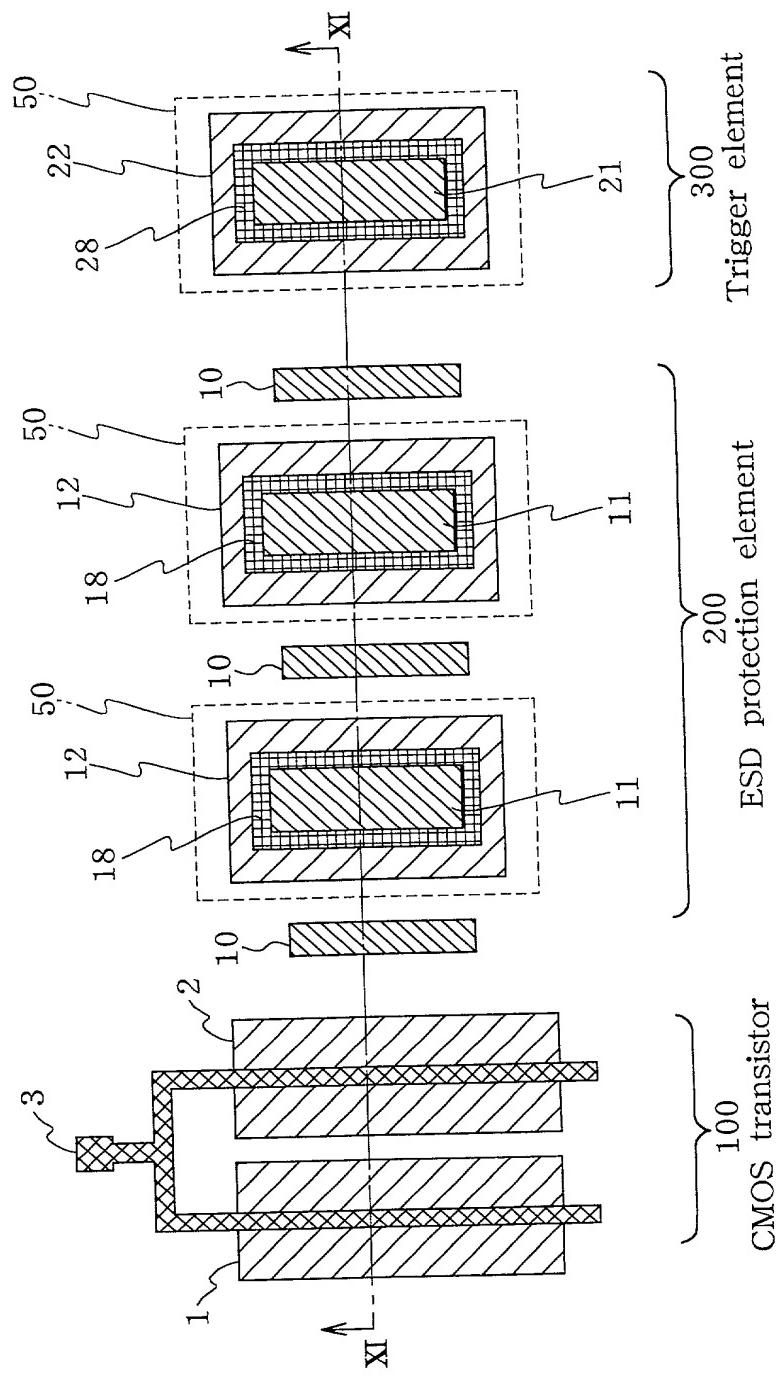
FIG.10

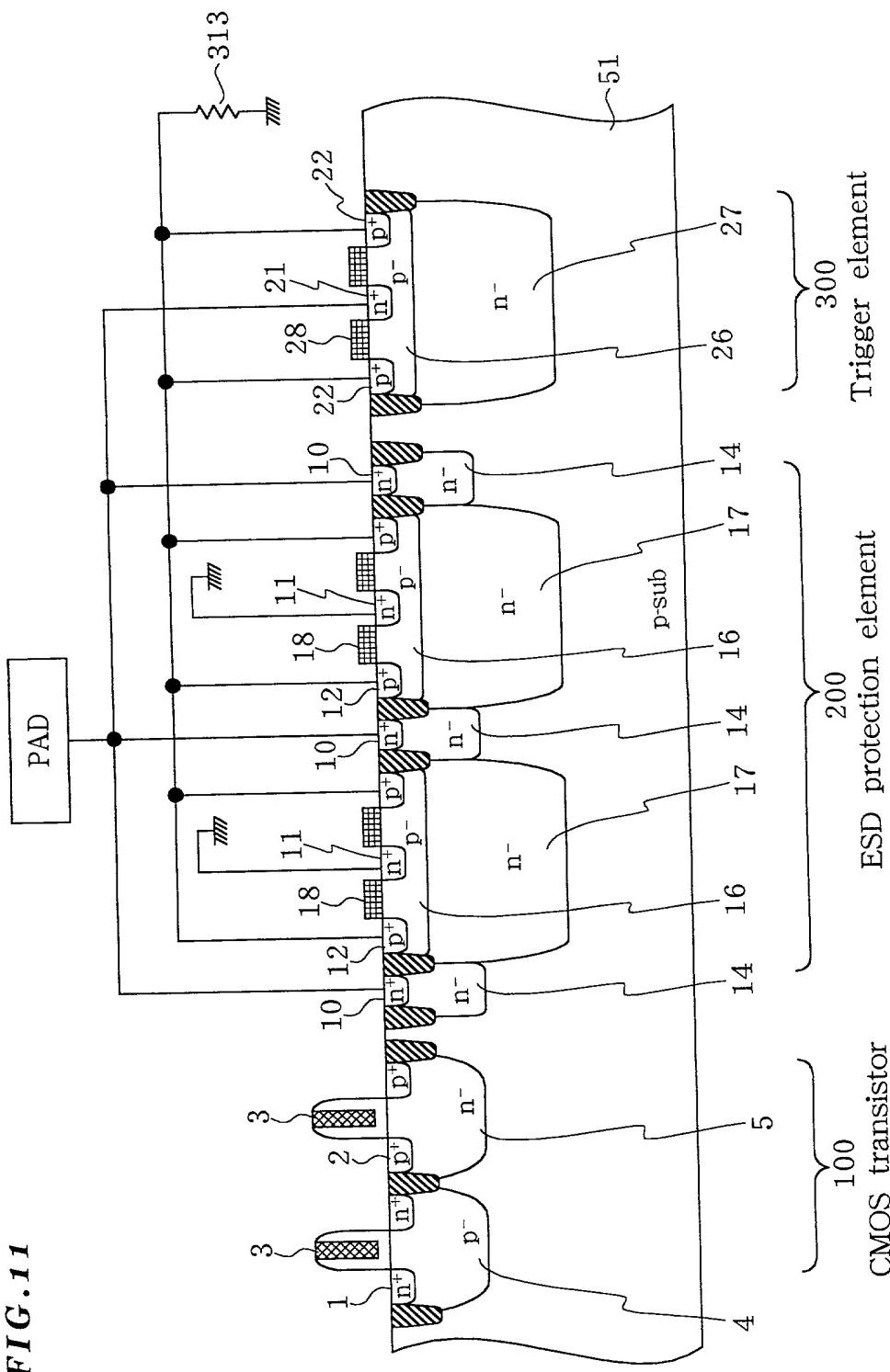
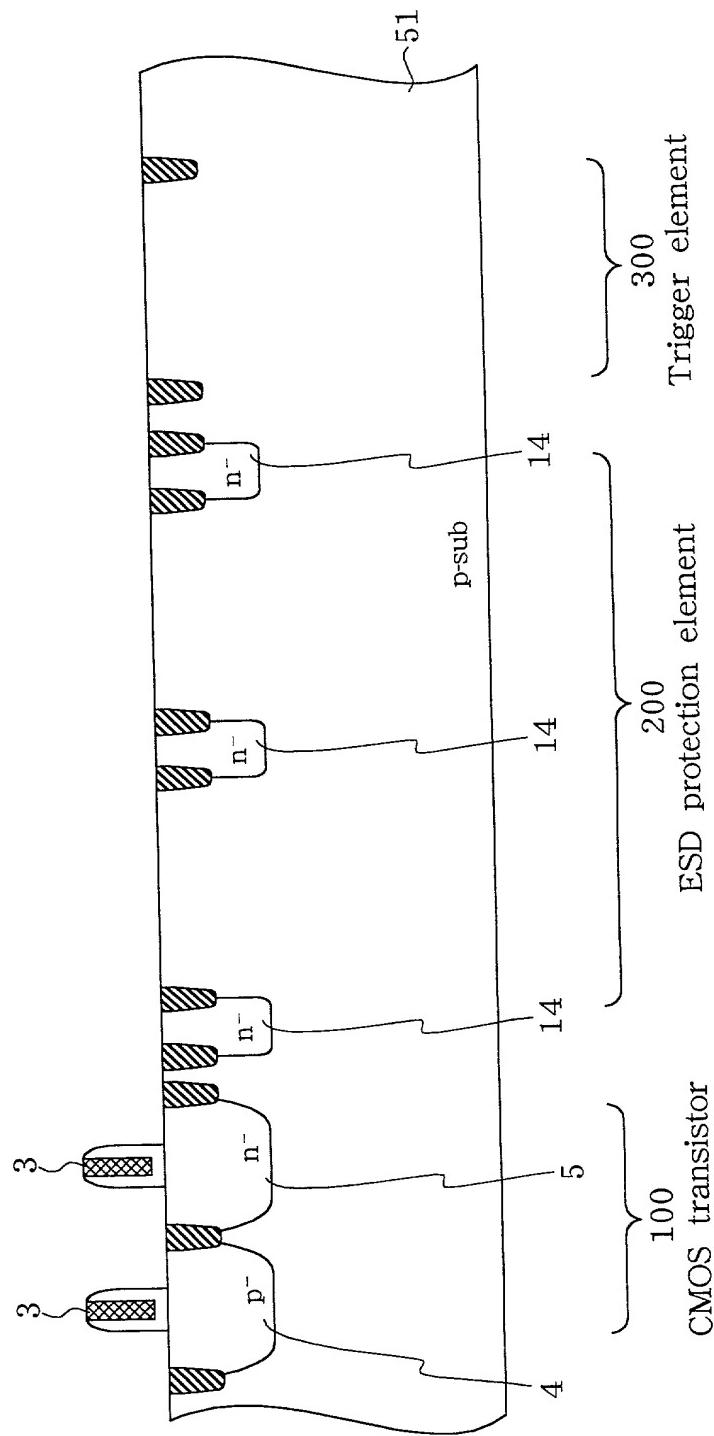
FIG. 11

FIG. 12

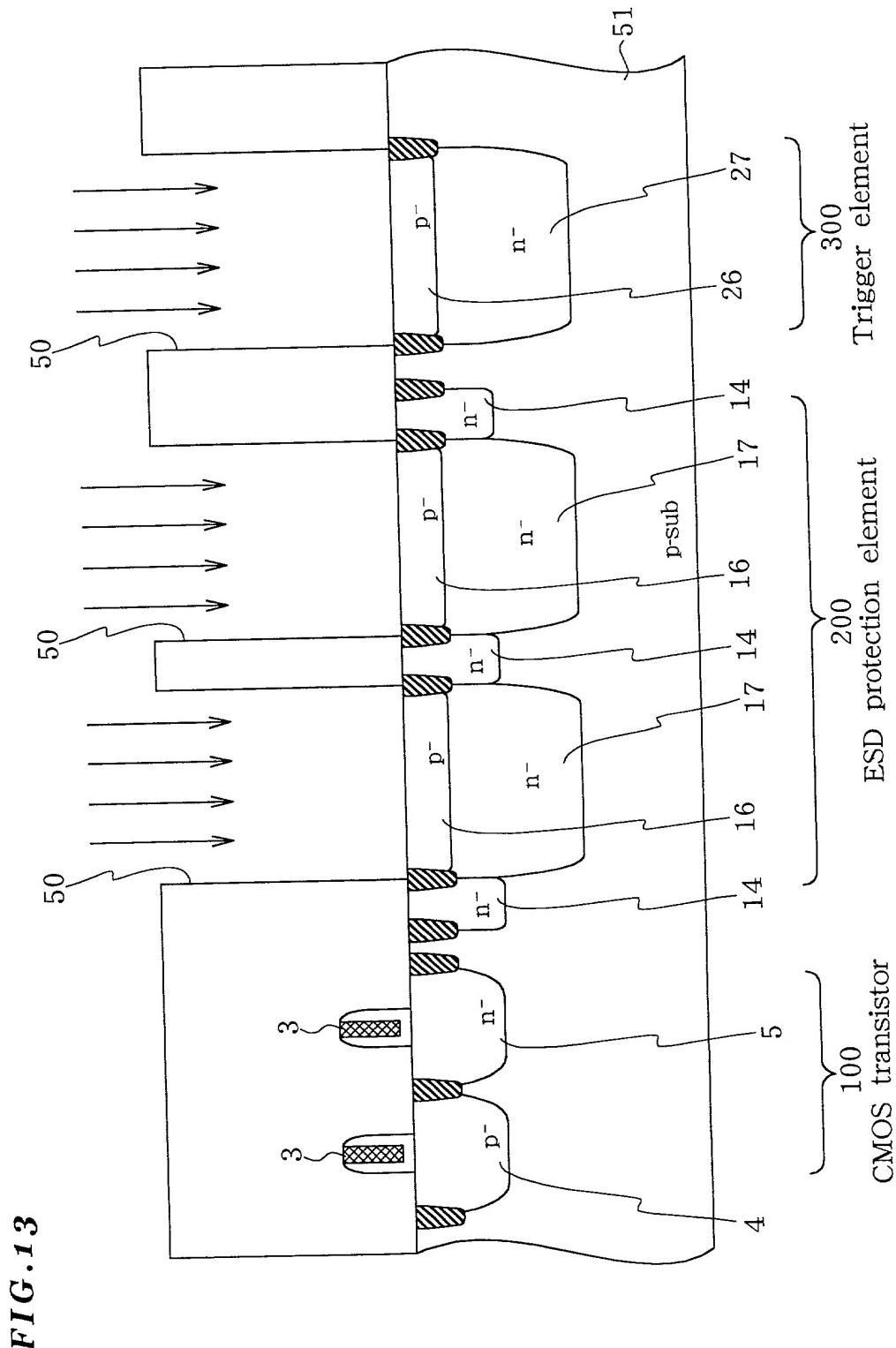
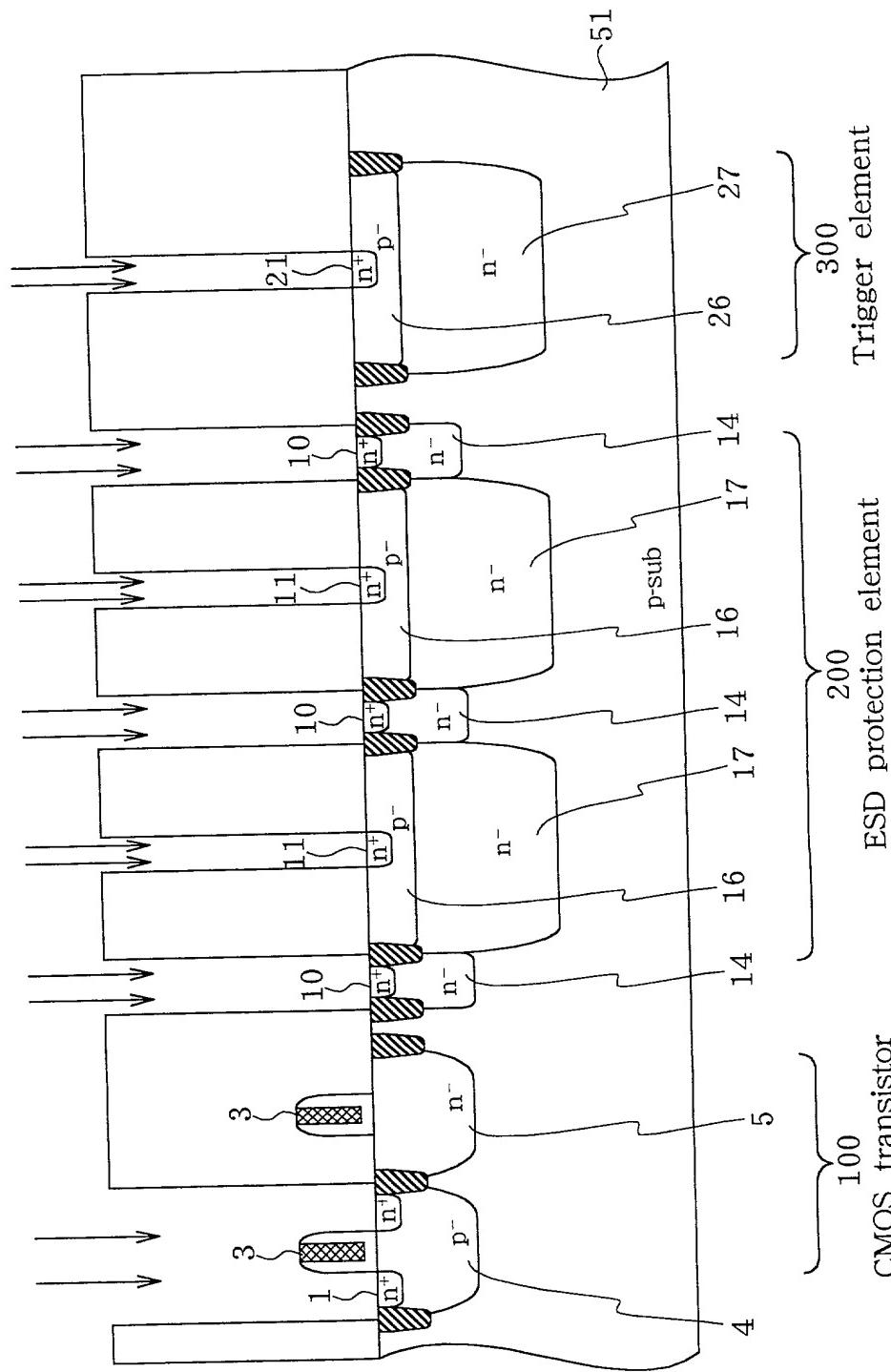


FIG. 13

FIG. 14



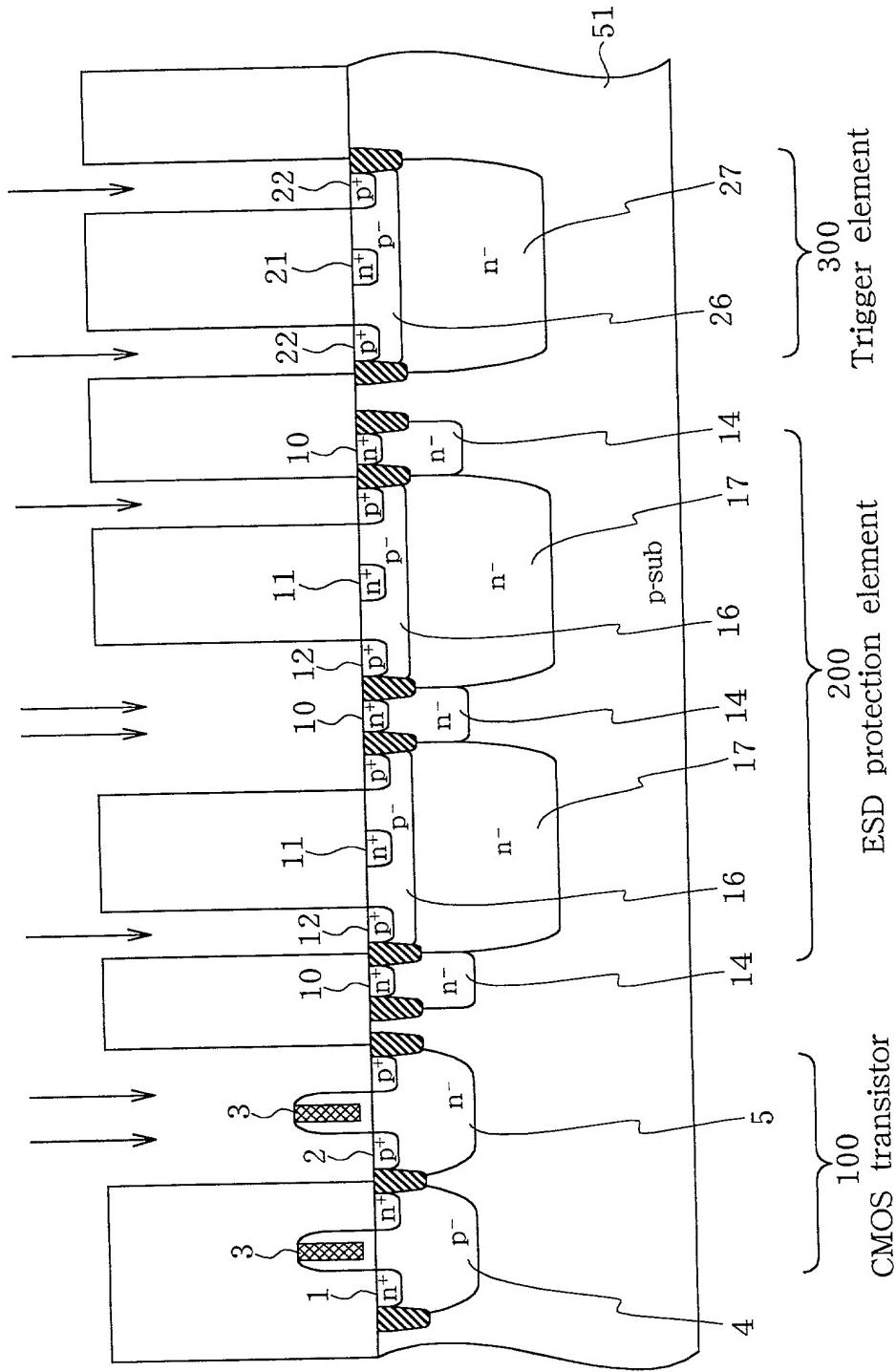


FIG. 15

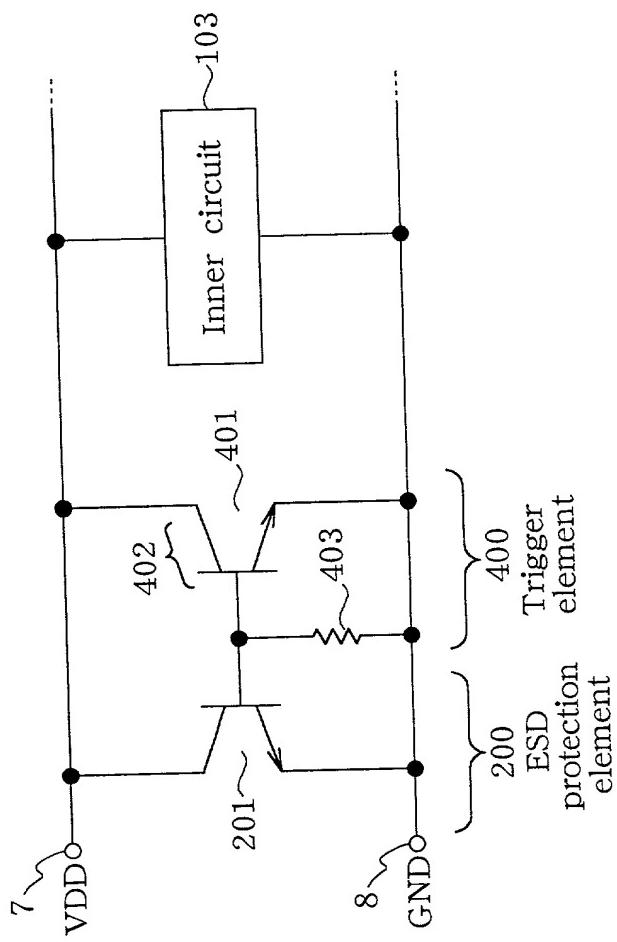


FIG. 16

FIG. 17

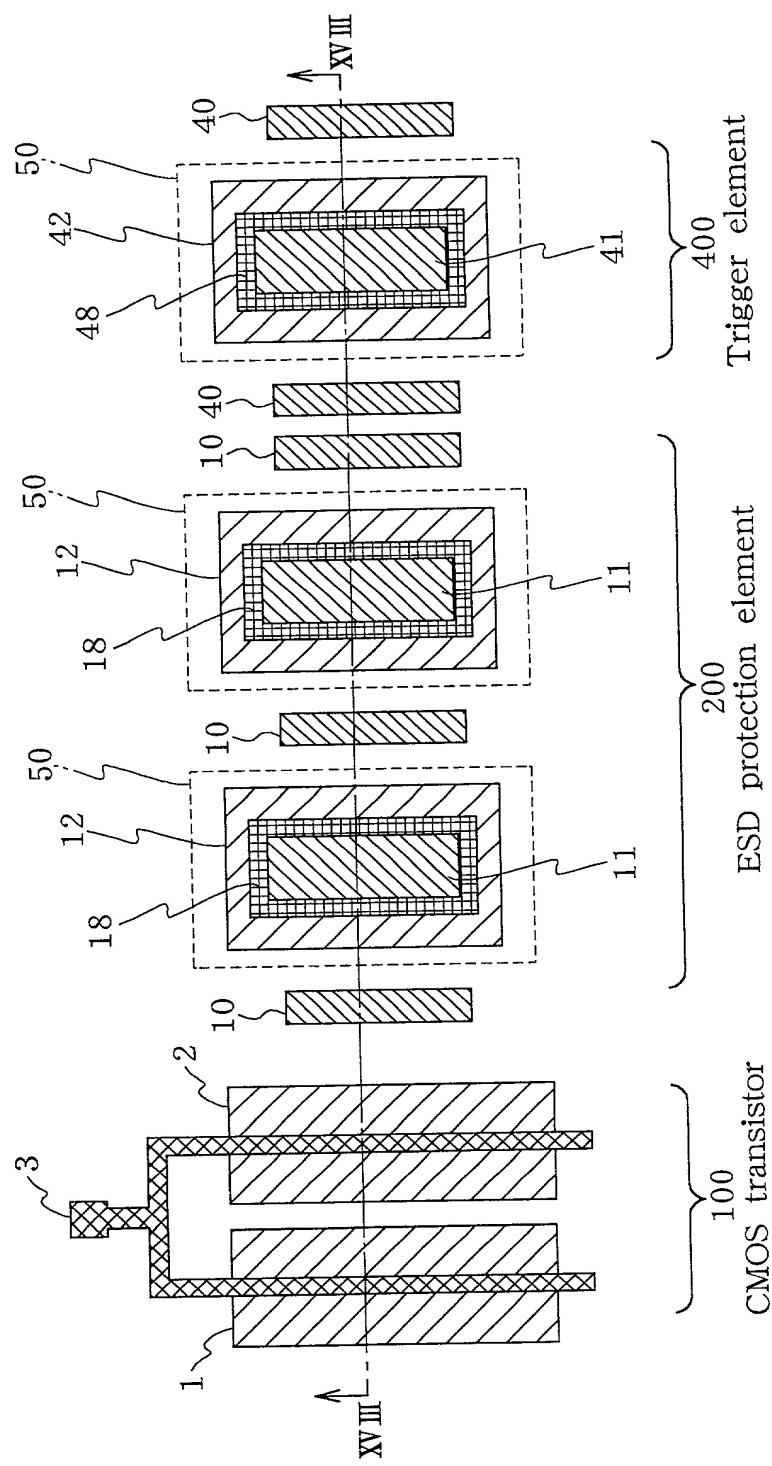
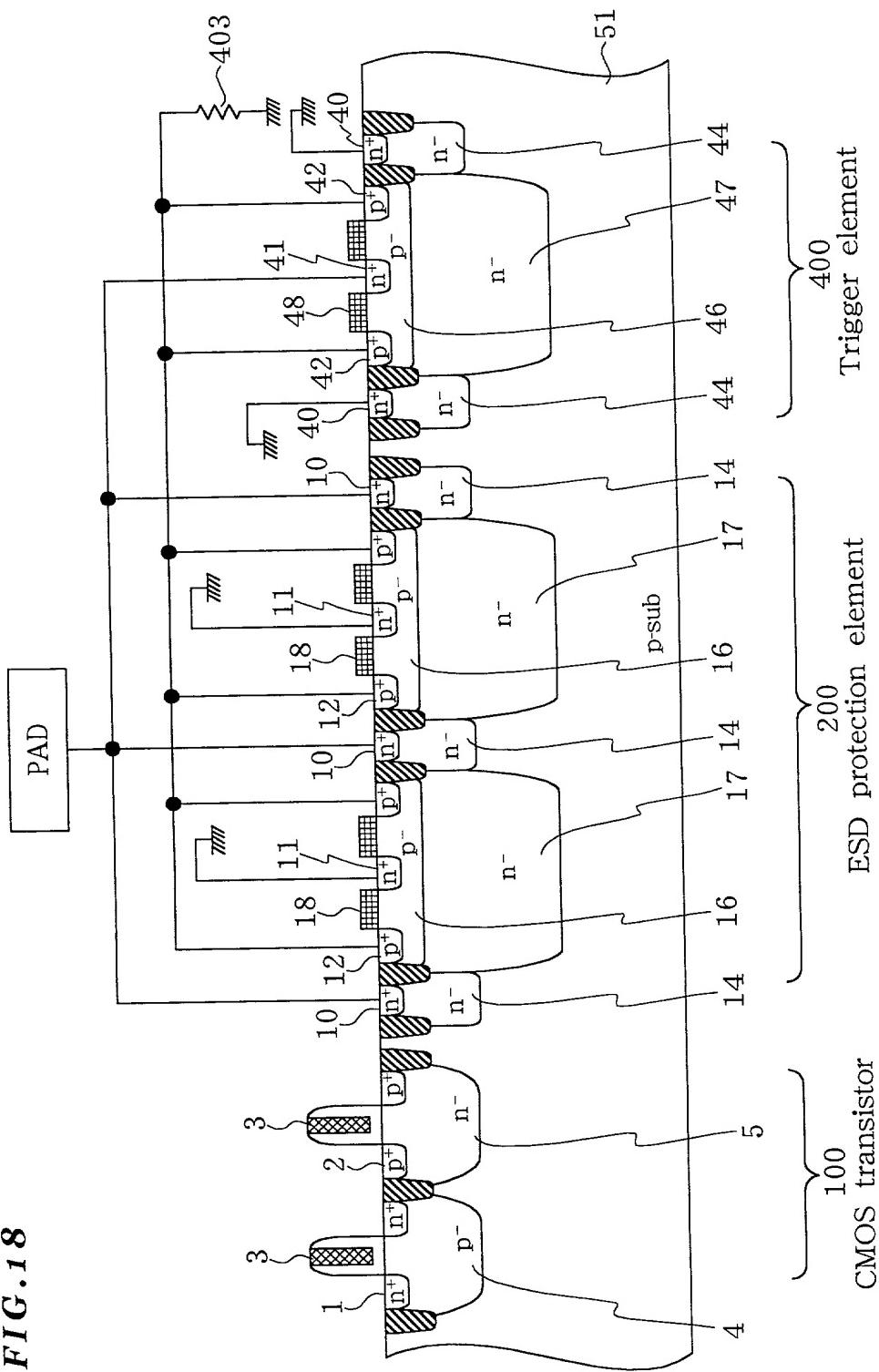


FIG. 1.8

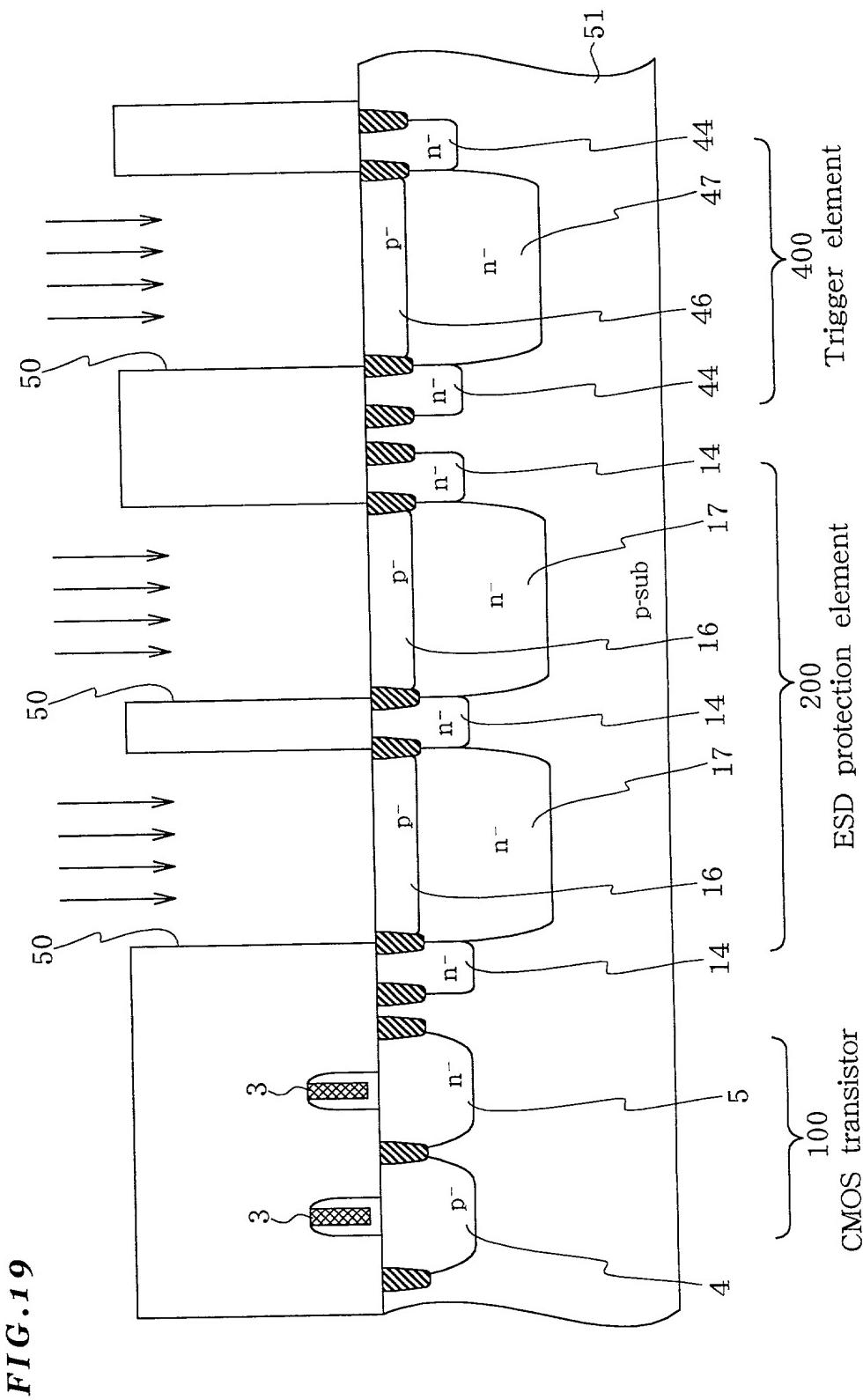


FIG. 20

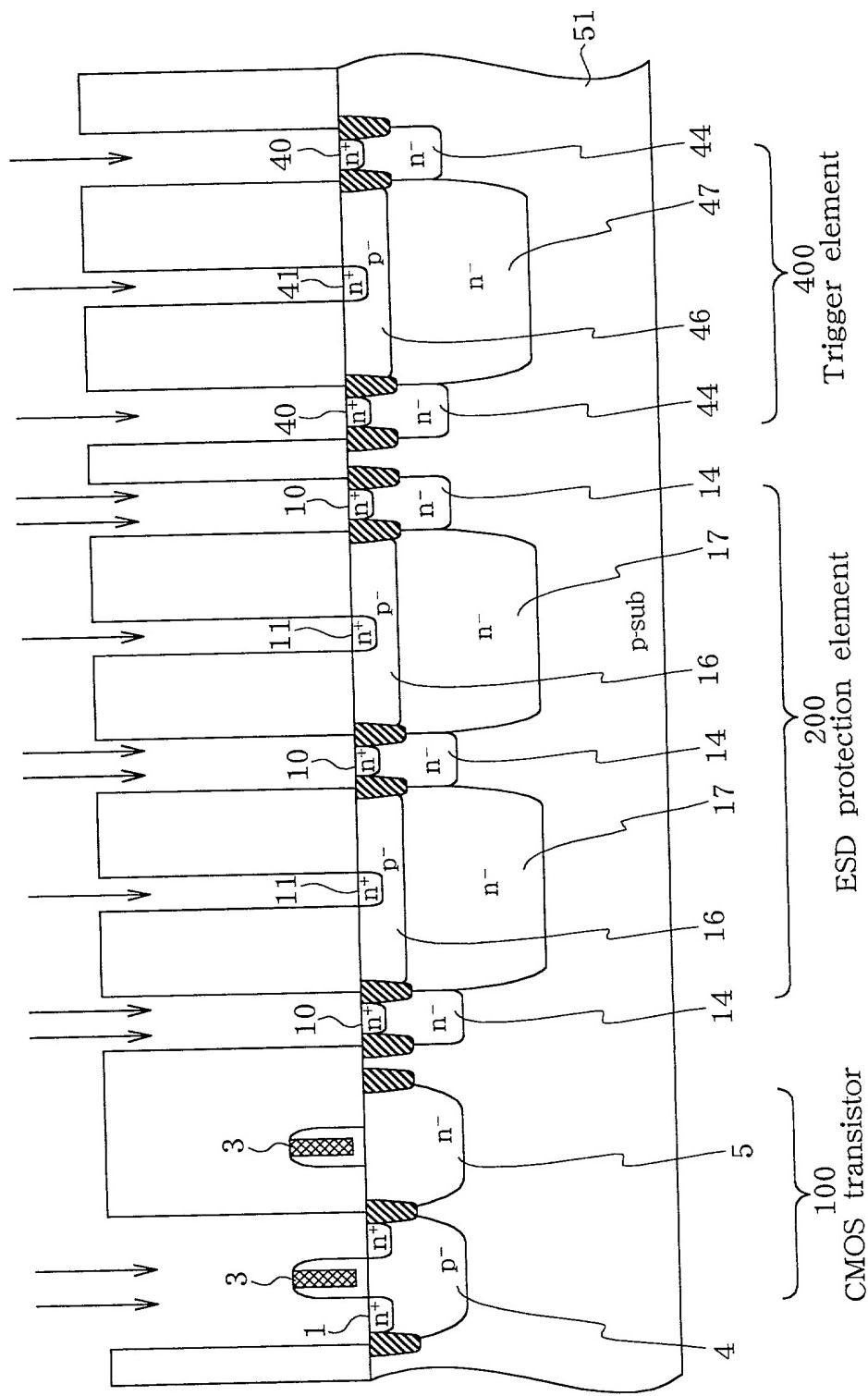
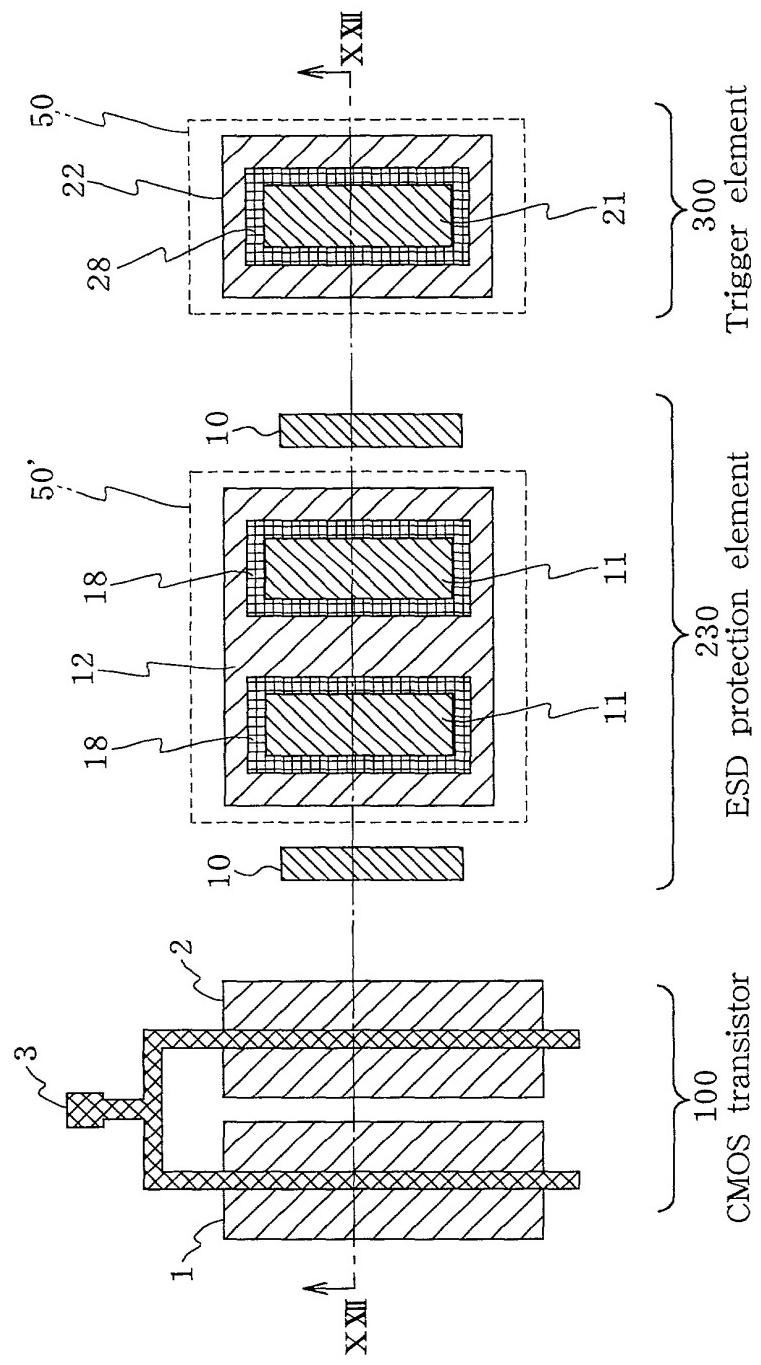


FIG. 21



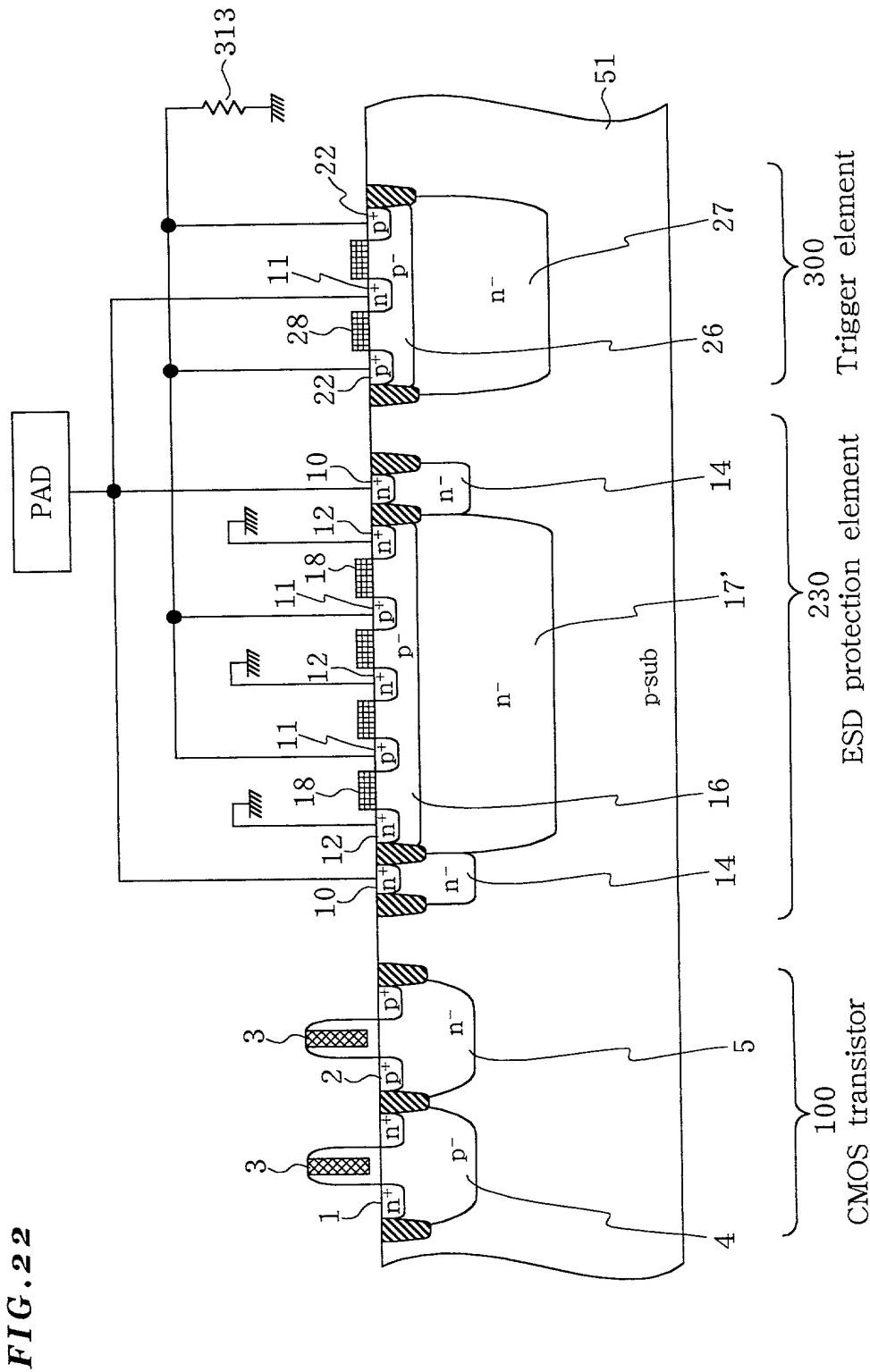


FIG. 23

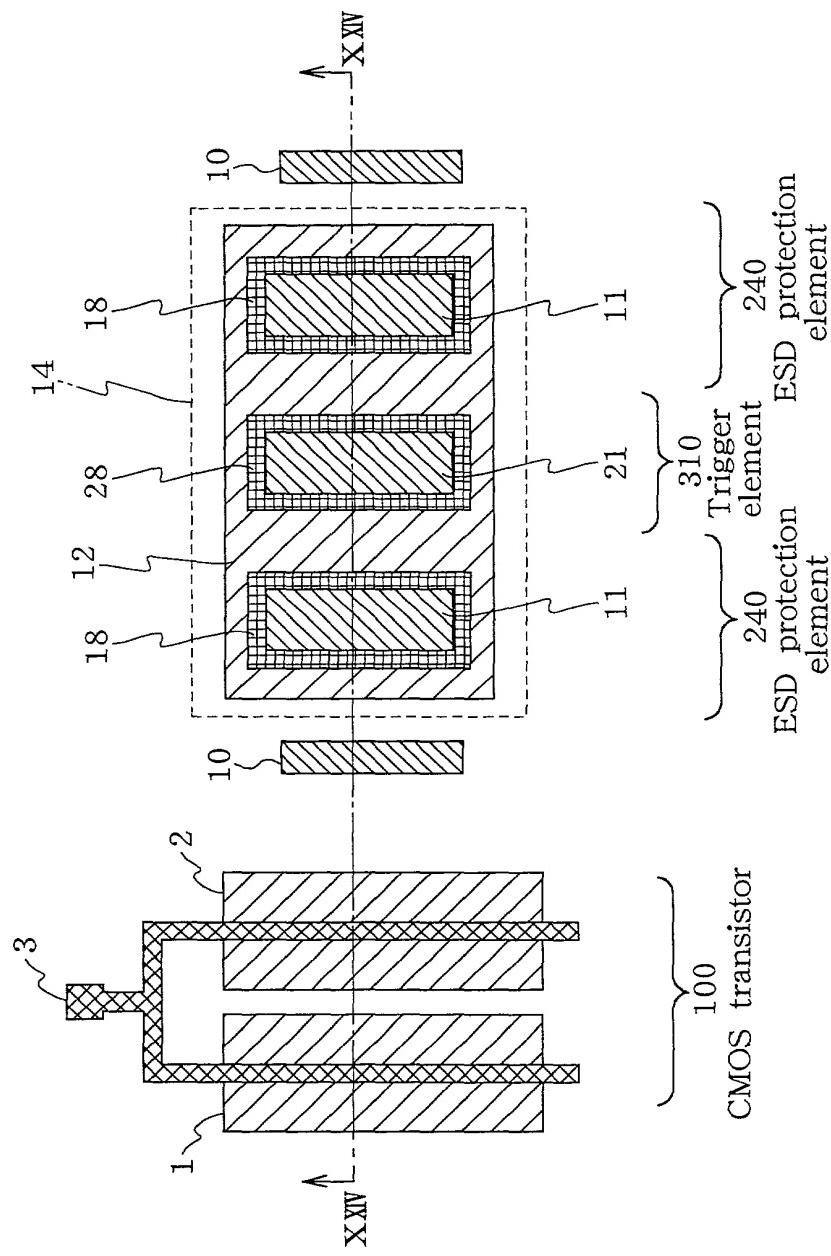


FIG. 24

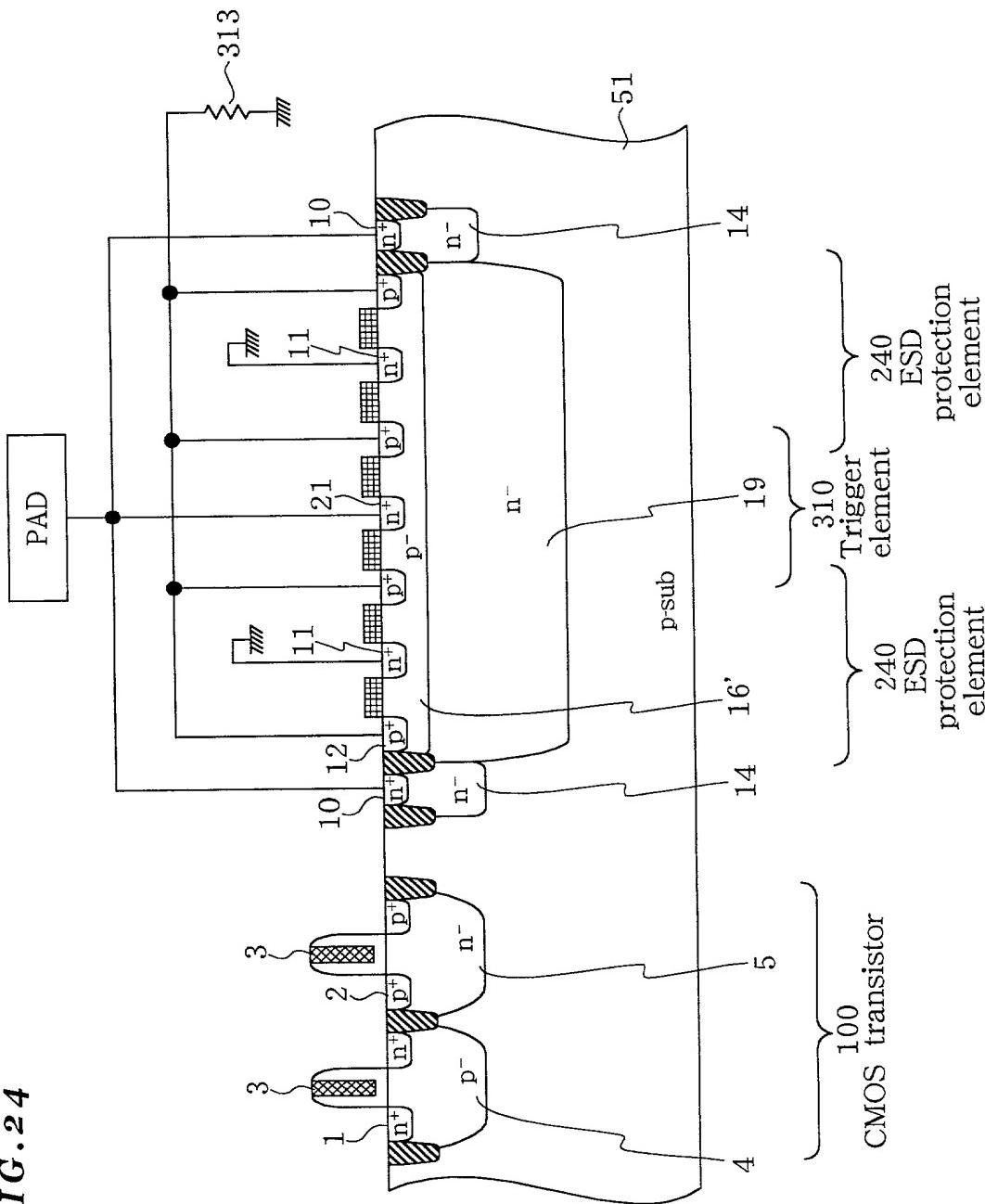


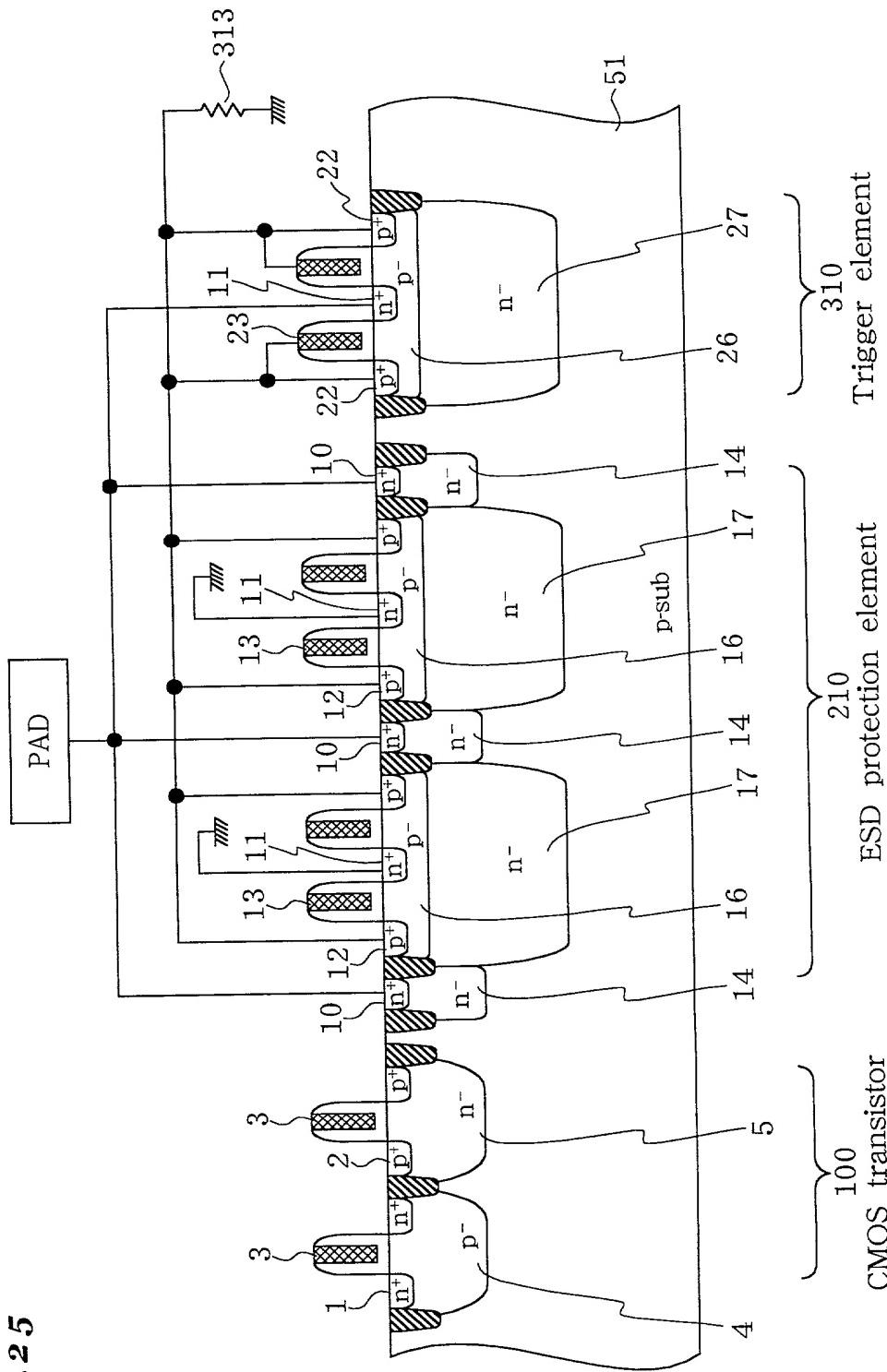
FIG. 25

FIG. 26

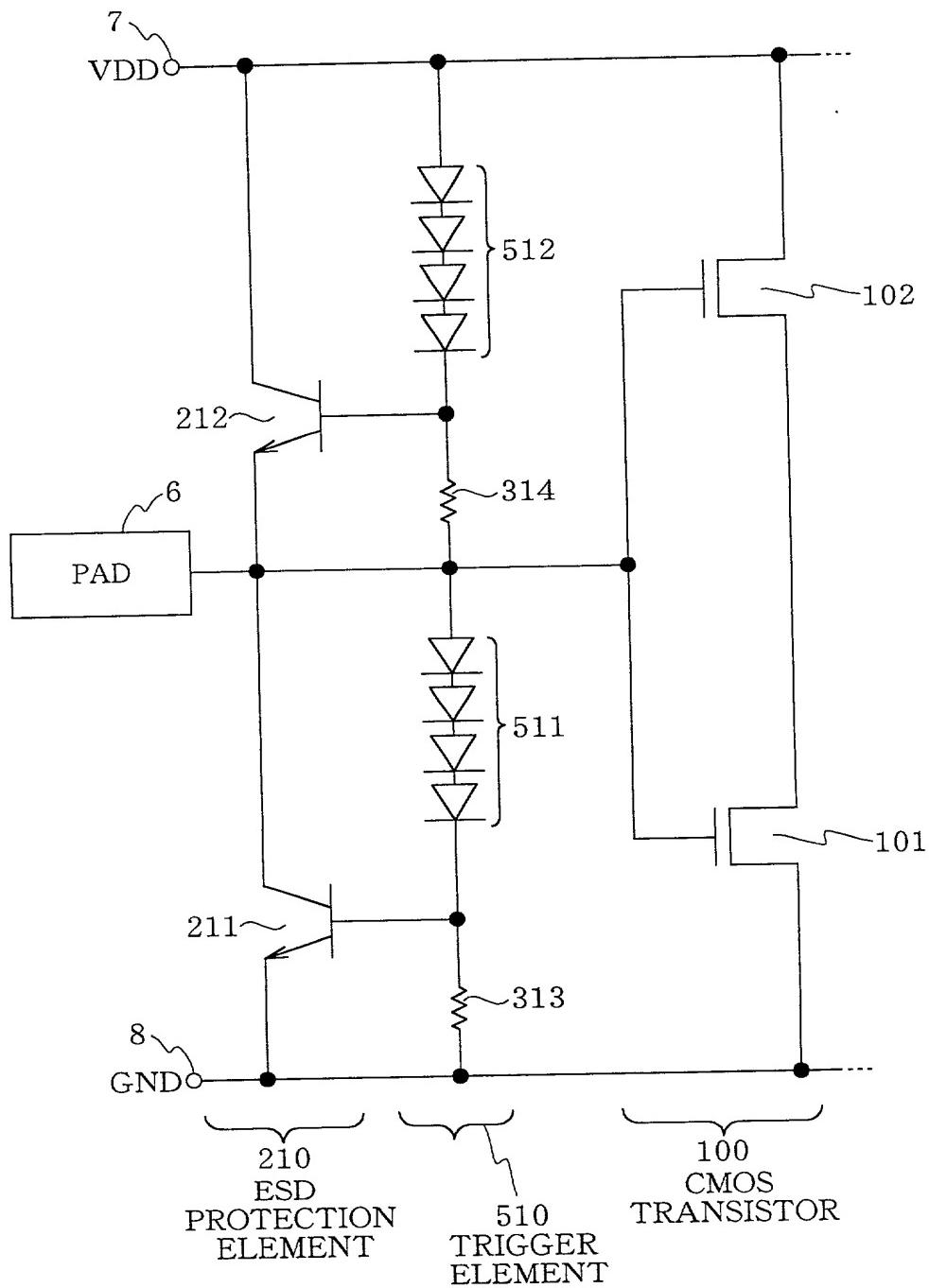


FIG. 27

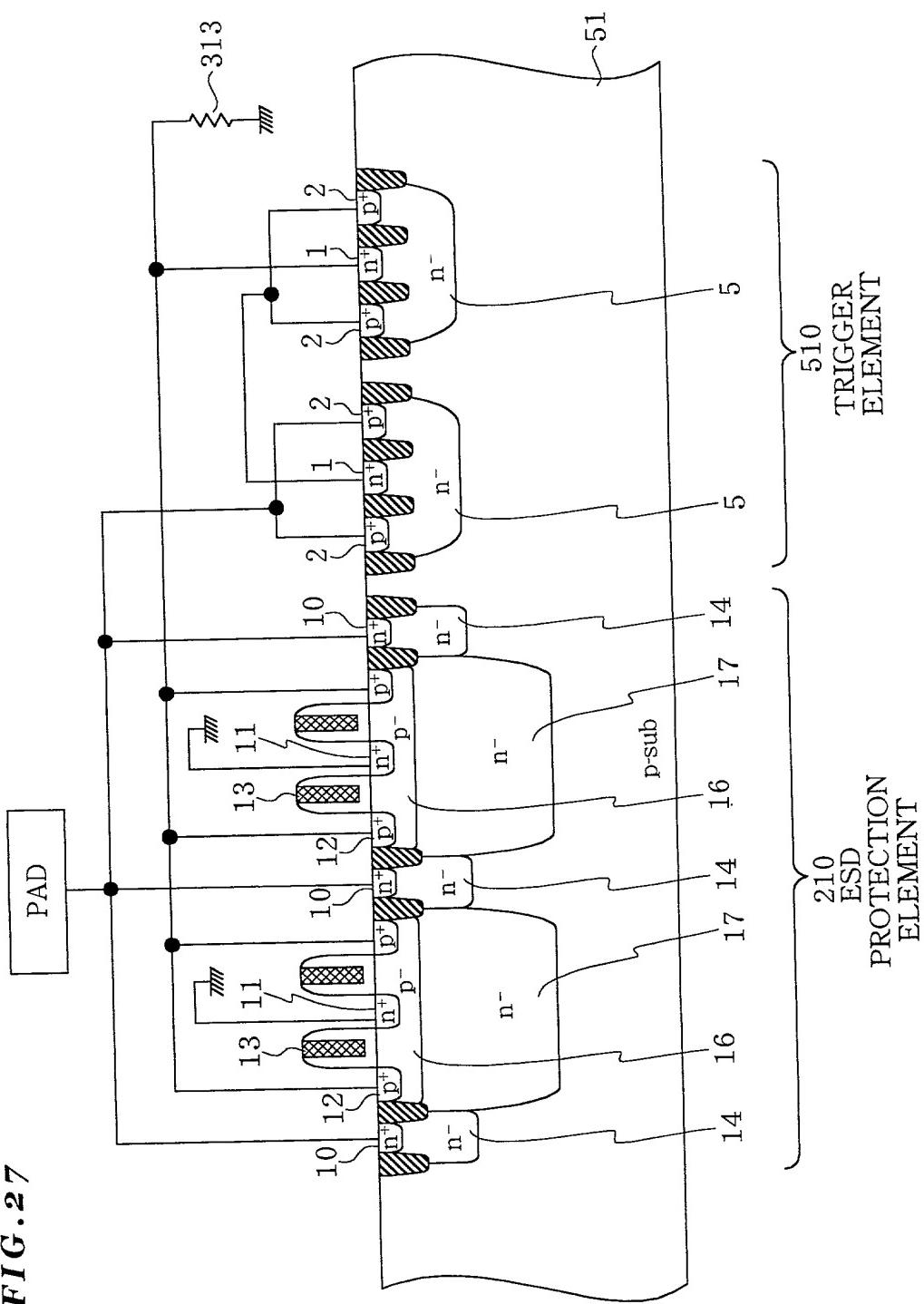
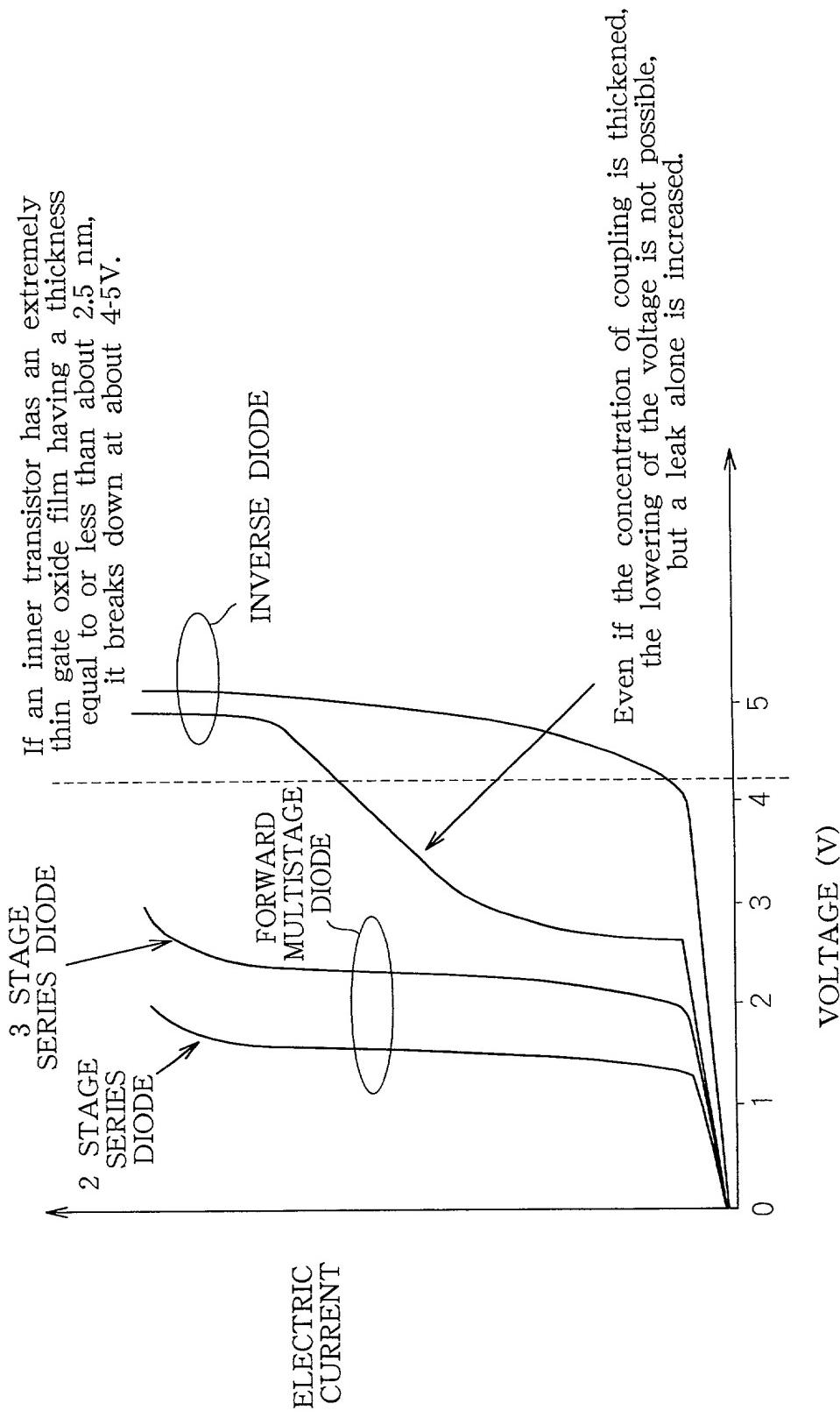
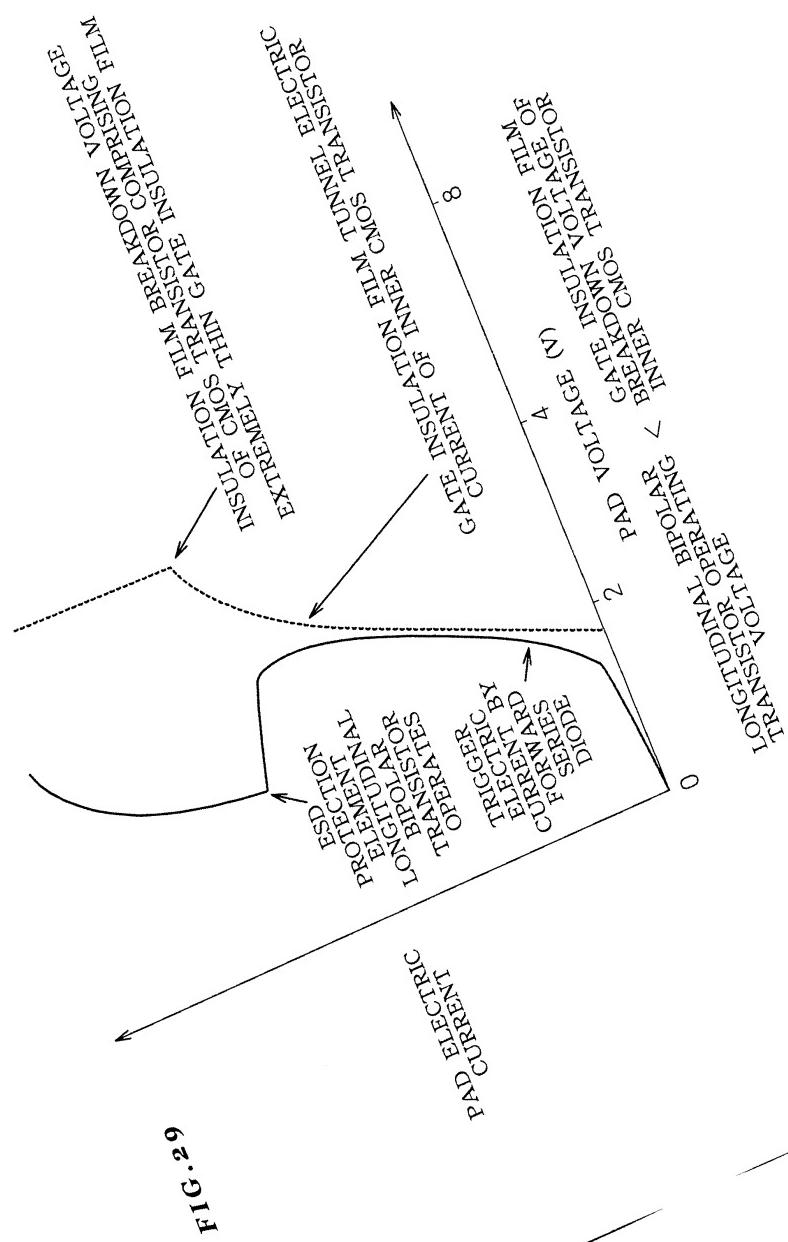


FIG. 28

COMPARISON OF FORWARD SERIES CONNECTION DIODE
AND INVERSE DIODE





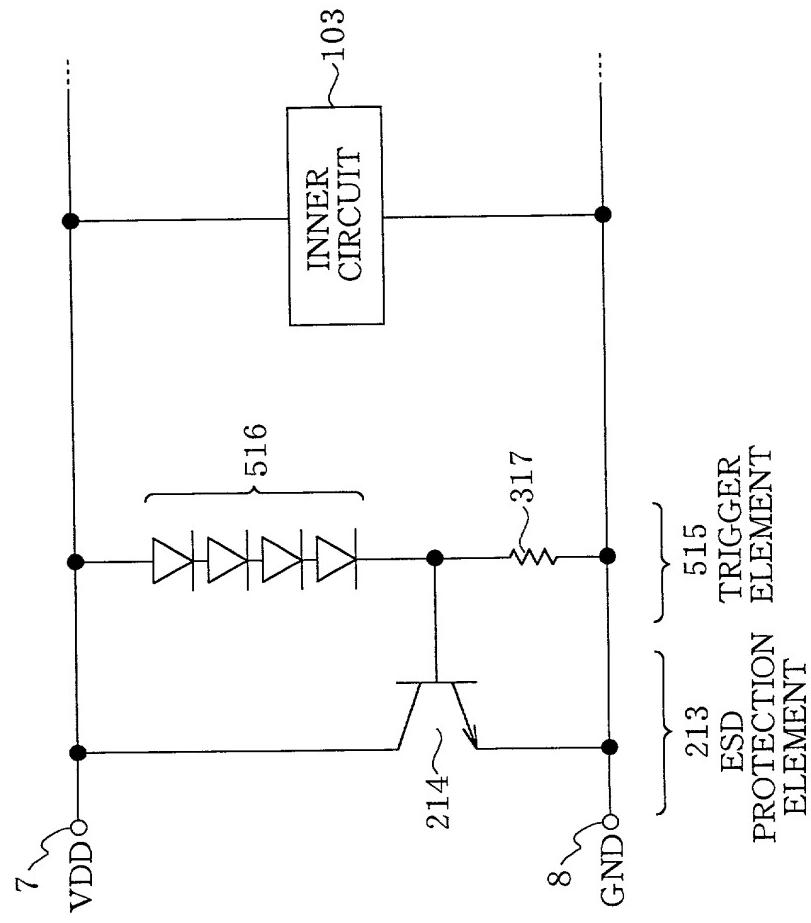


FIG. 30

FIG. 31

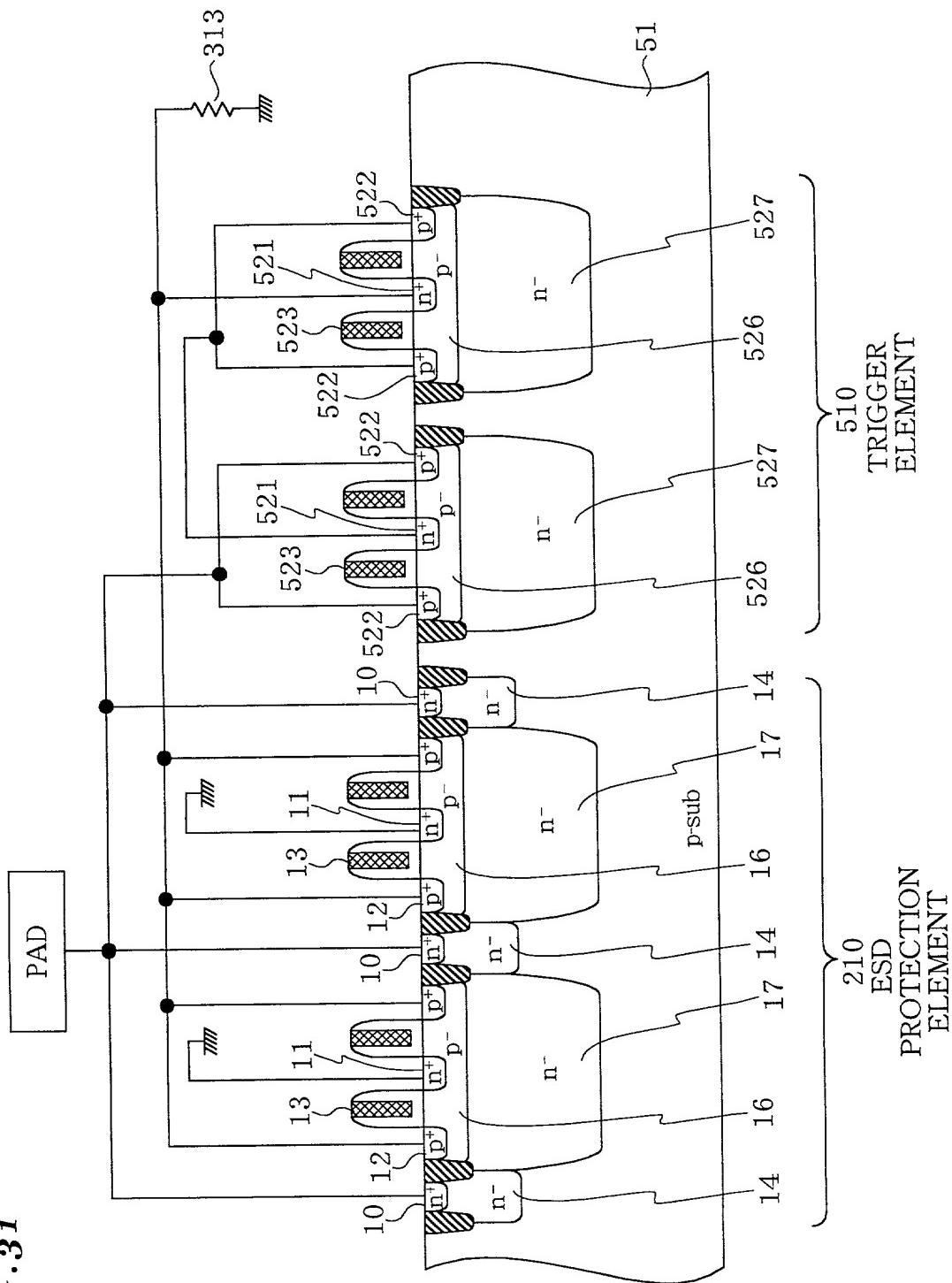


FIG. 32(a)
DIODE COMPRISING
P+LAYER/n WELL
FABRICATED BY
EXISTING CMOS PROCESS

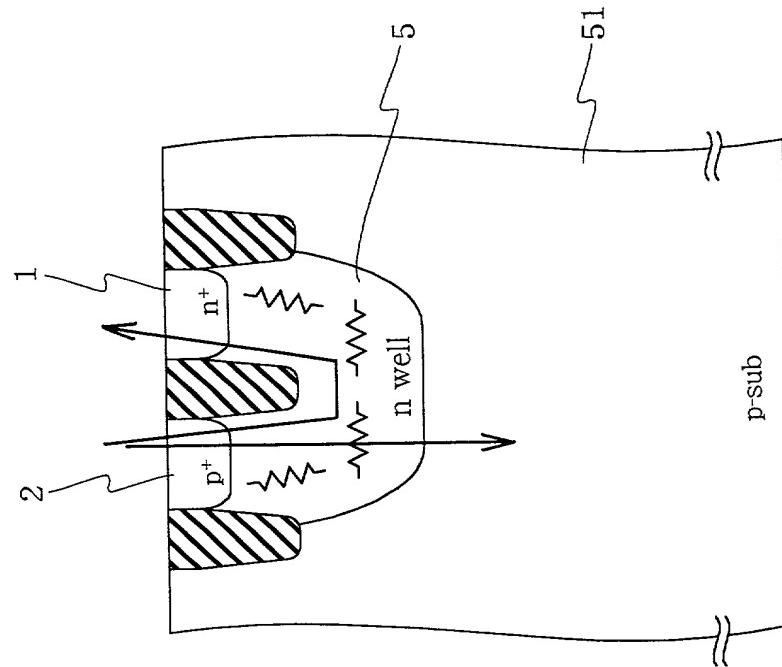


FIG. 32(b)

DIODE UTILIZING ONE PORTION
OF LONGITUDINAL
BIPOLAR TRANSISTOR

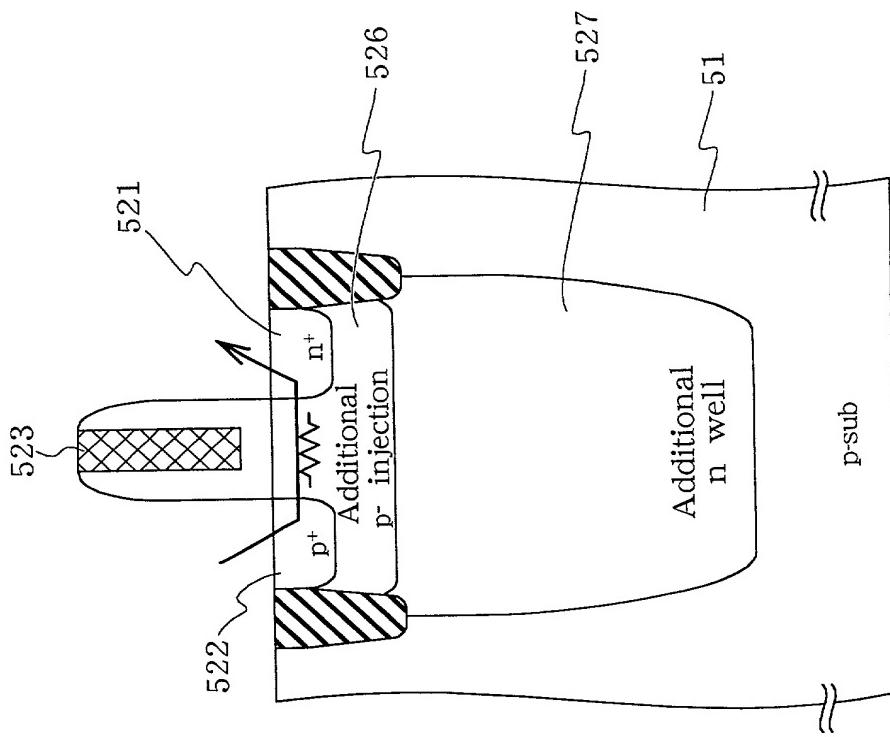
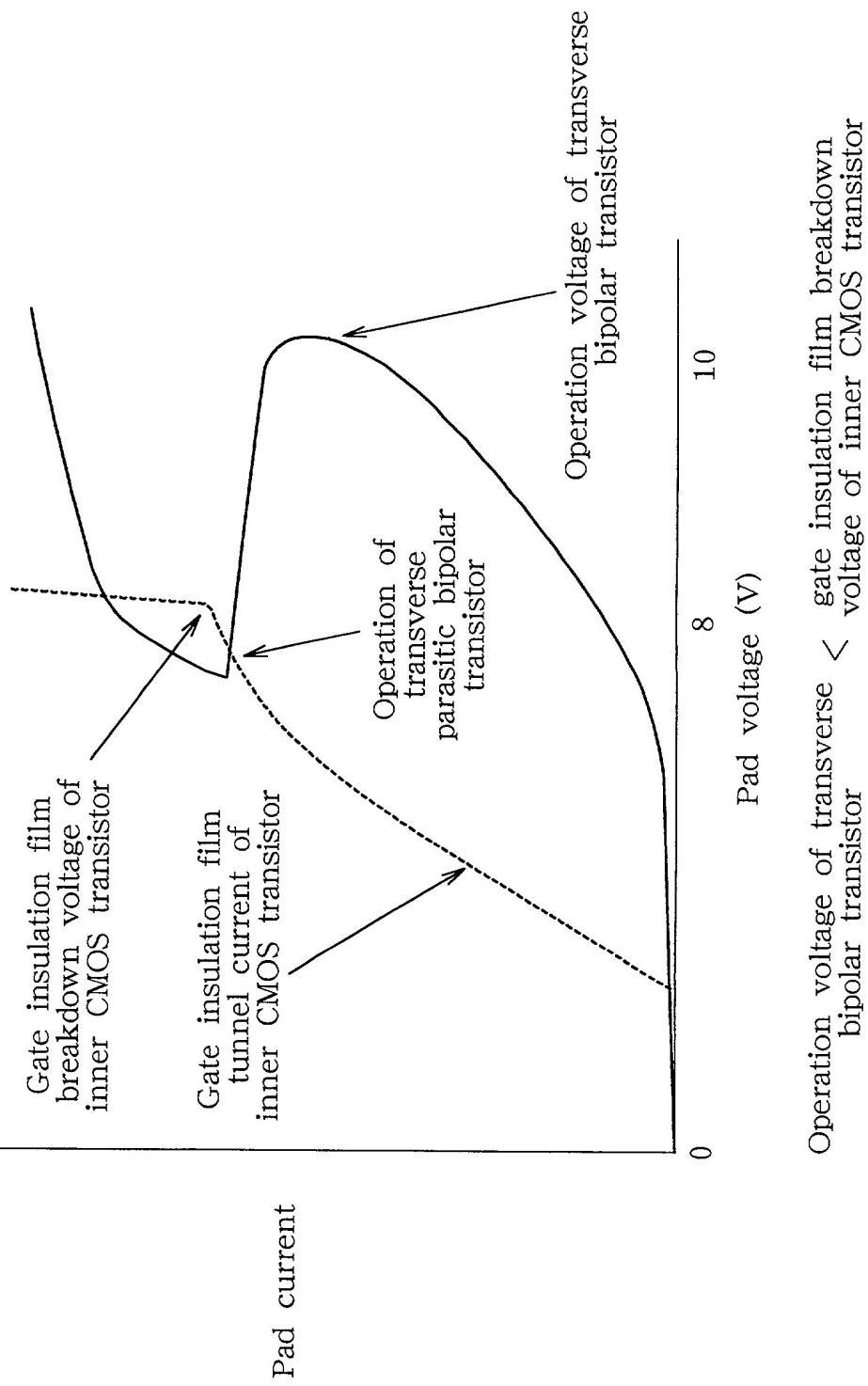


FIG. 33

Operation voltage of transverse bipolar transistor < gate insulation film breakdown voltage of inner CMOS transistor